

COVER SHEET	1
BLOCK DIAGRAM	2
GPIO & JUMPER SETTING	3
Intel LGA775-CPU	4-6
nVidia - MCP73	7-15
DDR II DIMM 1and DIMM2 1 & 2	16-17
VGA & HDMI & DVI CONNECTOR	18
LAN - Realtek RTL8211BL	19
USB CONNECTORS	20
SIO-ITE 8718F	21
IDE & SATA& COM1& COM2& LPT	22
FAN & TPM	23
Azalia CODEC(ALC888S)	24
IEEE1394 VIA VT6308P	25
MS7 ACPI Controller	26
FSB_VTT & NB_1P3V	27
VRM11 Intersil 6312 3Phase	28
PCI EXPRESS X16 & X 1 SLOT	29
PCI Slot 1 & 2	30
ATX & Front Panel	31
Audio De-Pop Circuit	32
Auto BOM manual	33
CLOCK DISTRIBUTION CHART	34
POWER DELIVERY CHART	35
POWER SEQUENCE	36

# MS-7399

Version 1.0

## CPU:

Intel Prescott ( L2=2MB )  
 Intel Cendar Mill (65nm)  
 Intel Smithfield (90nm Dual core)  
 Intel Presler (65nm Dual core)  
 Intel Conroe (65nm Dual core)  
 Intel Kentsfield  
 Intel Yorkfield  
 Intel Wolfdale

## System Chipset:

nVidia - MCP73PV/S

## On Board Chipset:

BIOS -- SPI FLASH 4Mb  
 Azalia CODEC(ALC 888S)  
 LPC Super I/O -- ITE8718F  
 LAN-Realtek RTL8211BL  
 IEEE1394 -- VIA VT6308P

## Main Memory:

DDR II \* 2 (Max 2GB)

## Expansion Slots:

PCI Express X16 SLOT \* 1  
 PCI Express X1 SLOT \* 1  
 PCI 2.3 SLOT \* 2

## Intersil PWM:

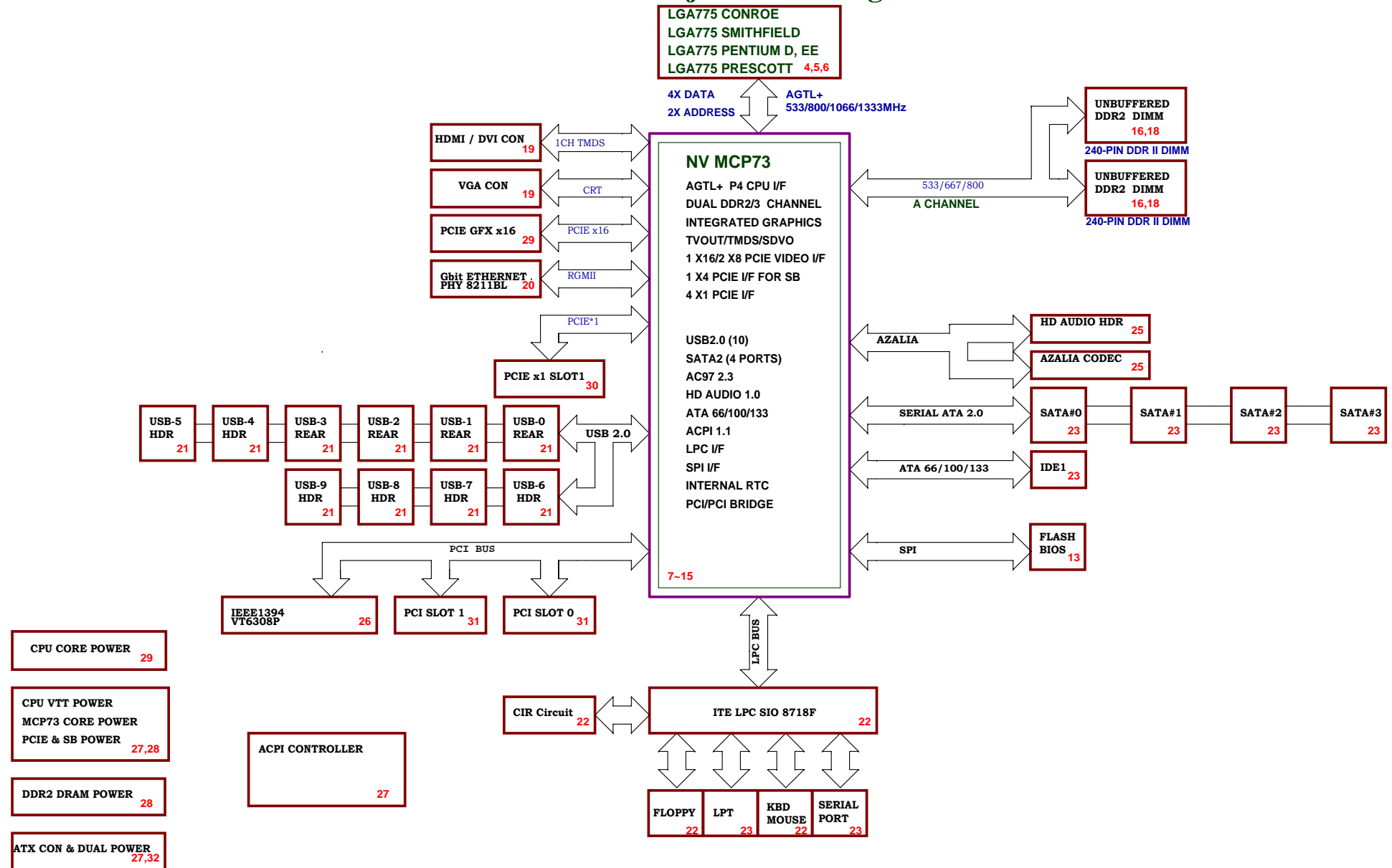
Controller: Intersil 6312 3 Phase



Persian Project

Aspire M1640  
 DVI + 1394

# acer Persian Project Block Diagram



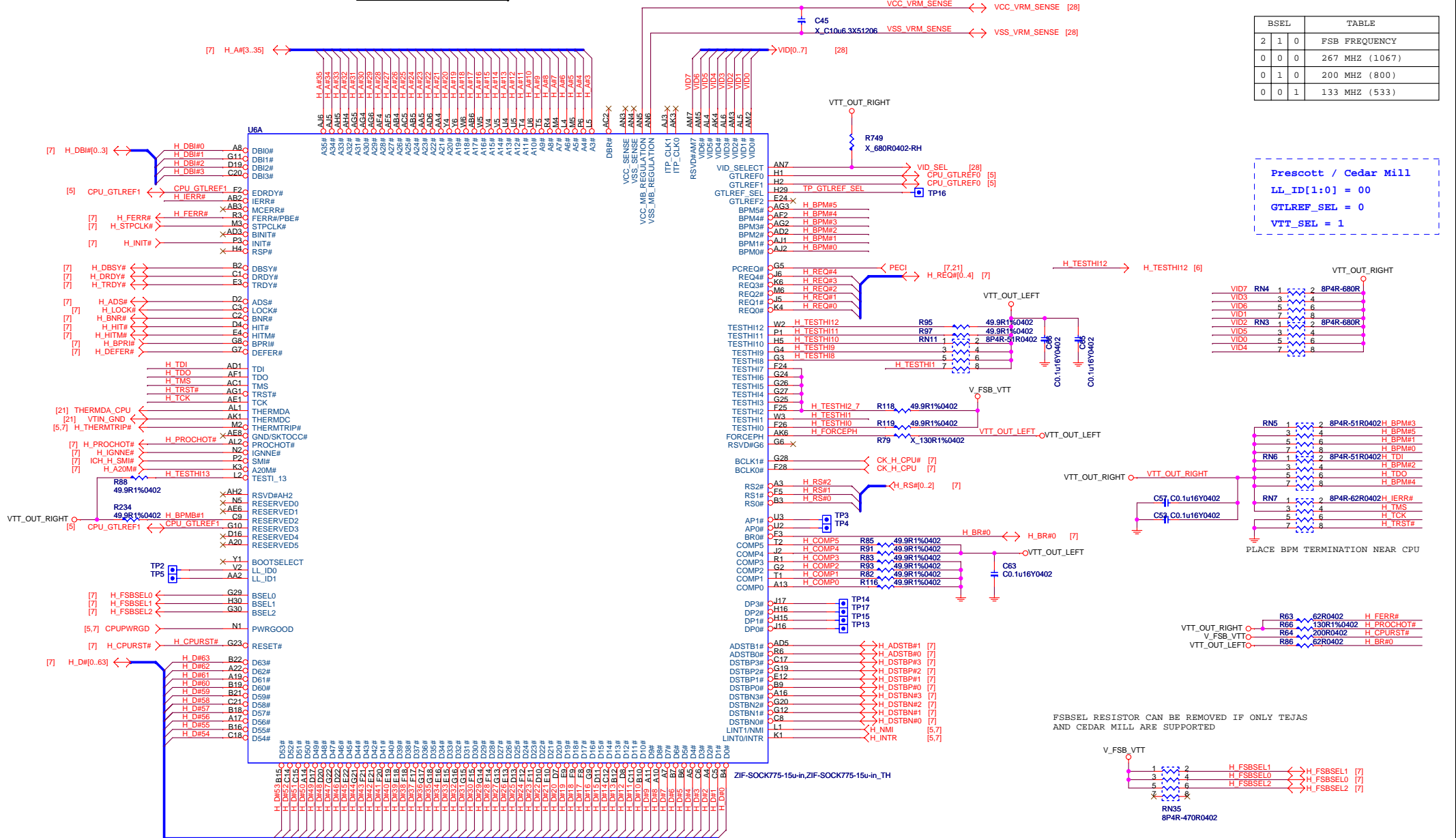
## MCP73 GPIO Config.

GPIO Pin	Type	Primary State
GPIO_2/NMI/PS2_CLK0	I/O(S5_3.3V)	<b>TMDS_DET1</b>
GPIO_3/SMI#/PS2_DATA0	I/O(S5_3.3V)	<b>TMDS_DET2</b>
GPIO_4/SCI/INTR/PS2_CLK1	I/O(S5_3.3V)	Unused
GPIO_5/INIT#/PS2_DATA1	I/O(S5_3.3V)	<b>OBR1</b>
GPIO_6/FERR#/SYS_SERR#/IGPU_GPIO6	I/O(S5_3.3V)	Unused
GPIO_7/NFERR#/SYS_PERR#/IGPU_GPIO7	I/O(S5_3.3V)	Unused
GPIO_8/SPI_DI	I/O(S5_3.3V)	Unused
GPIO_9/SPI_DO	I/O(S5_3.3V)	Unused
GPIO_10/SPI_CS0	I/O(S5_3.3V)	Unused
GPIO_11/SPI_CLK	I/O(S5_3.3V)	Unused
LPC_DRQ1#/GPIO_19/FANRPM1	I/O(3.3V)	Unused
PROCHOT#/GPIO_20	I/O(CPU_VTT)	<b>H_PROCHOT#</b>
PE_WAKE#/GPIO_21	I/O(S5_3.3V)	<b>WAKE#</b>
HDA_SDATA_IN0/GPIO_22	I/O(S5_3.3V)	<b>HDA_SDATA_IN</b>
HDA_SDATA_IN1/GPIO_23/MGPIO_0	I/O(S5_3.3V)	Unused
HDA_SDATA_IN2/GPIO_24/MGPIO_2	I/O(3.3V)	Unused
USB_OC0#/GPIO_25	I/O(S5_3.3V)	<b>OC#1</b>
USB_OC1#/GPIO_26	I/O(S5_3.3V)	<b>OC#2</b>
USB_OC2#/GPIO_27	I/O(S5_3.3V)	<b>OC#3</b>
USB_OC3#/GPIO_28	I/O(S5_3.3V)	<b>Pull Hi</b>
USB_OC4#/GPIO_29	I/O(S5_3.3V)	<b>Pull Hi</b>
PCI_PME#/GPIO_30	I/O(S5_3.3V)	<b>PCI_PME#</b>
SIO_PME#/GPIO_31	I/O(S5_3.3V)	<b>SIO_PME#</b>
EXT_SMI#/GPIO_32	I/O(S5_3.3V)	<b>LPC_SMI#</b>
SUS_CLK/GPIO_34	I/O(S5_3.3V)	Unused
MII0_INTR/GPIO_35	I/O(S5_3.3V)	<b>RGMI0_INTR#</b>
MII0_PXER/GPIO_36/PWR_LED#	I/O(S5_3.3V)	<b>RGMI0_RX_ER</b>
MII0_PWRDWN/GPIO_37	I/O(S5_3.3V)	<b>RGMI0_PREDN</b>
PCI_REQ3#/GPIO_38/RS232_CTS#	I/O(3.3V)	<b>PREQ#3</b>
PCI_GNT3#/GPIO_39/RS232_RTS#	I/O(3.3V)	Unused
PCI_REQ2#/GPIO_40/RS232_DSR#	I/O(3.3V)	<b>PREQ#2</b>
PCI_GNT2#/GPIO_41/RS232_DTR#	I/O(3.3V)	<b>PGNT#2</b>
LPC_RESET#/GPIO_42	I/O(3.3V)	Unused
PCI_PERR#/GPIO_43/RS232_DCD#	I/O(3.3V)	<b>PERR#</b>
HDA_SYNC/GPIO_44	I/O(3.3V)	<b>AZ_SYNC_R</b>
HDA_SDATA_OUT/GPIO_45	I/O(3.3V)	<b>HDA_SDATA_OUT</b>
LPC_DRQ0#/GPIO_50	I/O(3.3V)	<b>LPC_DRQ#0</b>
PCI_REQ4#/GPIO52/RS232_SIN#	I/O(3.3V)	<b>PREQ#4</b>
PCI_GNT4#/GPIO_53/RS232_SOUT#	I/O(3.3V)	Unused
A20GATE/GPIO_55	I/O(3.3V)	<b>A20GATE</b>
KBRDRSTIN#/GPIO_56	I/O(3.3V)	<b>KBRST#</b>
SATA_LED#/GPIO_57	A(3.3V)	<b>SATALED#</b>
THERMTRIP#/GPIO_58	I/O(CPU_VTT)	<b>H_THERMTRIP#</b>
THERM#/GPIO_59	I/O(3.3V)	Unused
FANRPM0/GPIO_60	I/O(3.3V)	<b>OBR2</b>
FANCTL0/GPIO_61	I/O(3.3V)	<b>AUDIO_FRONT_IO</b>
FANCTL1/GPIO_62	I/O(3.3V)	<b>DEPOP_GPIO</b>
CABLE_DET_P/GPIO_63	I/O(3.3V)	<b>ATADETO</b>

## PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTX# PCI_INTY# PCI_INTZ# PCI_INTW#	PREQ#0 PGNT#0	AD21	PCICLK0
PCI Slot 2	PCI_INTY# PCI_INTZ# PCI_INTW# PCI_INTX#	PREQ#1 PGNT#1	AD22	PCICLK1
1394	PCI_INTW#	PREQ#2 PGNT#2	AD23	1394_PCLK

# CPU SIGNAL BLOCK



BSEL	TABLE
2 1 0	FSB FREQUENCY
0 0 0	267 MHZ (1067)
0 1 0	200 MHZ (800)
0 0 1	133 MHZ (533)

Prescott / Cedar Mill

LL\_ID[1:0] = 00

GTLREF\_SEL = 0

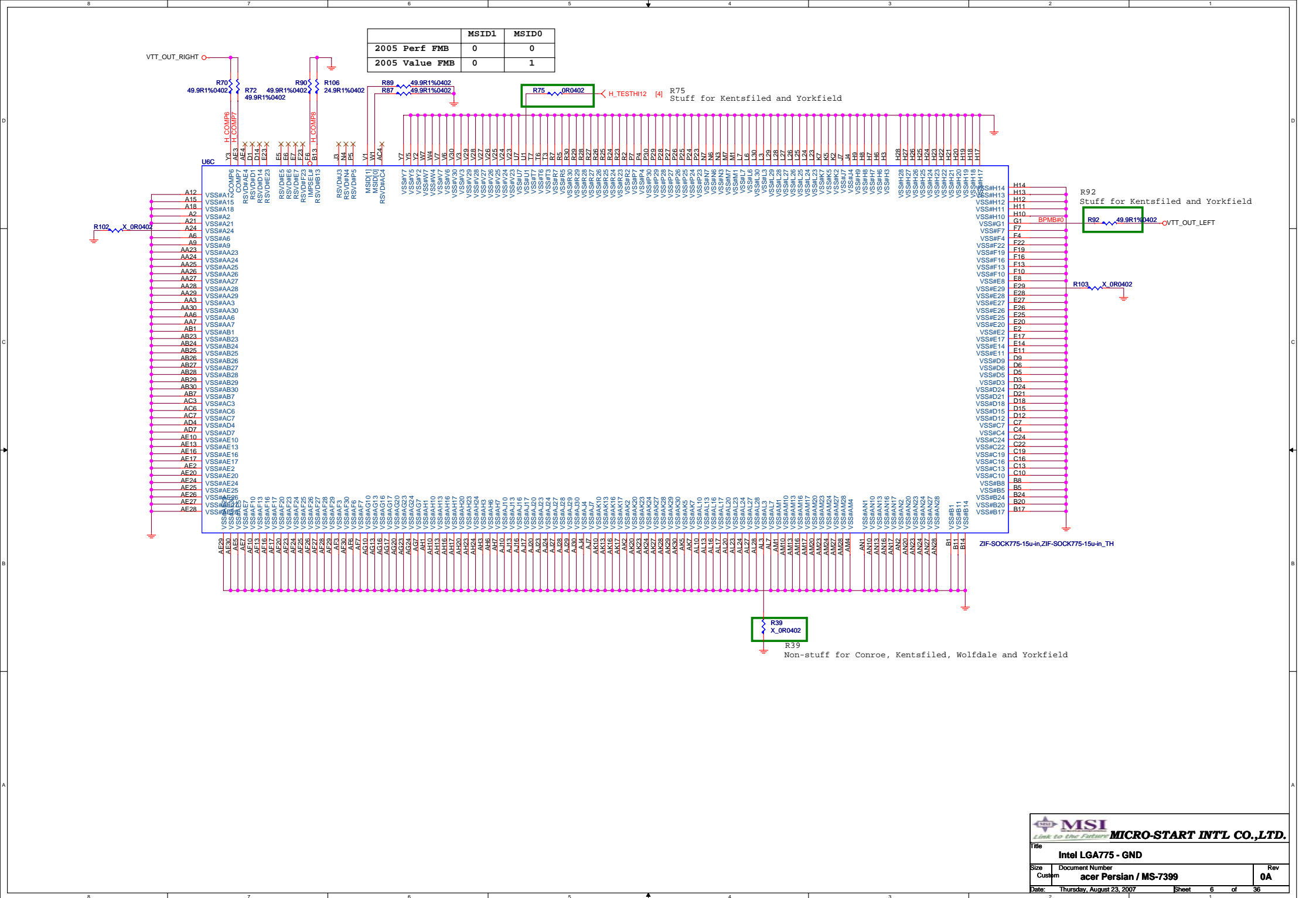
VTT\_SEL = 1

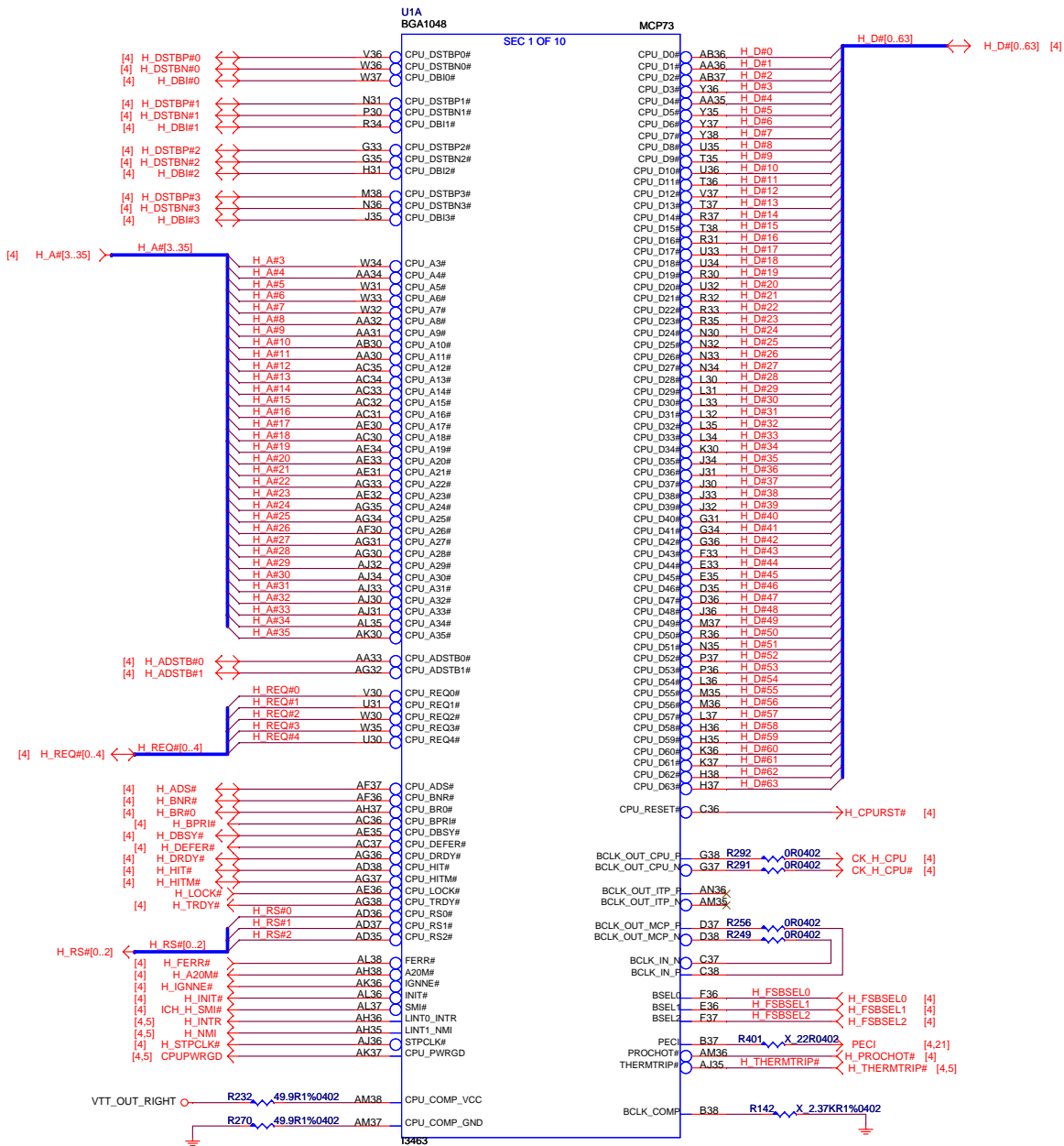
FSBSEL RESISTOR CAN BE REMOVED IF ONLY TEJAS AND CEDAR MILL ARE SUPPORTED

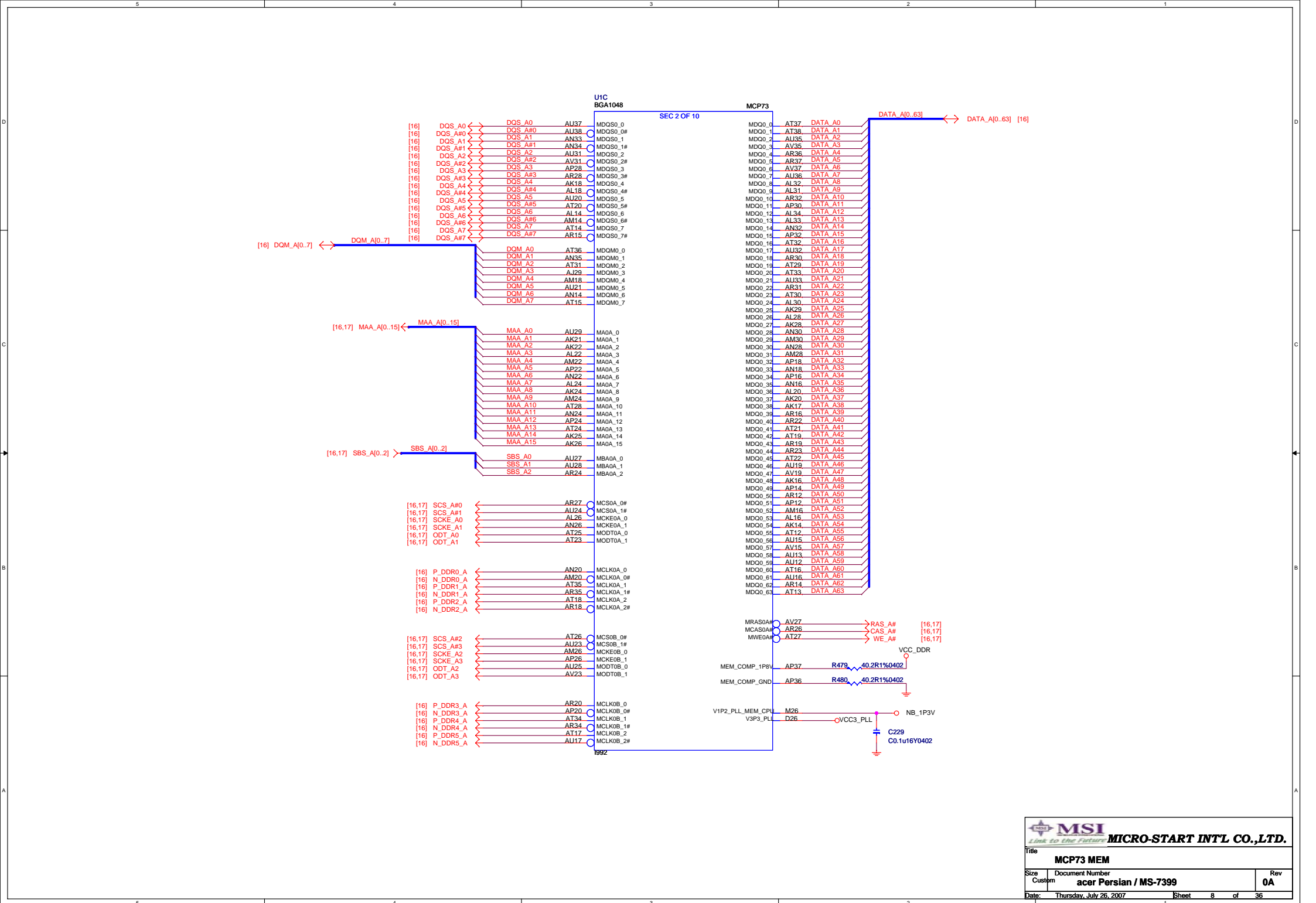


Intel LGA775 - Signals		
Size	Document Number	Rev
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Date:	Thursday, August 23, 2007	Sheet 4 of 36



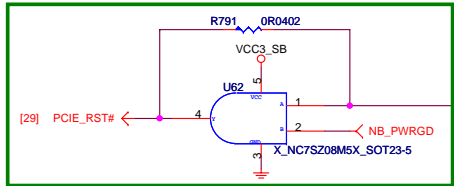




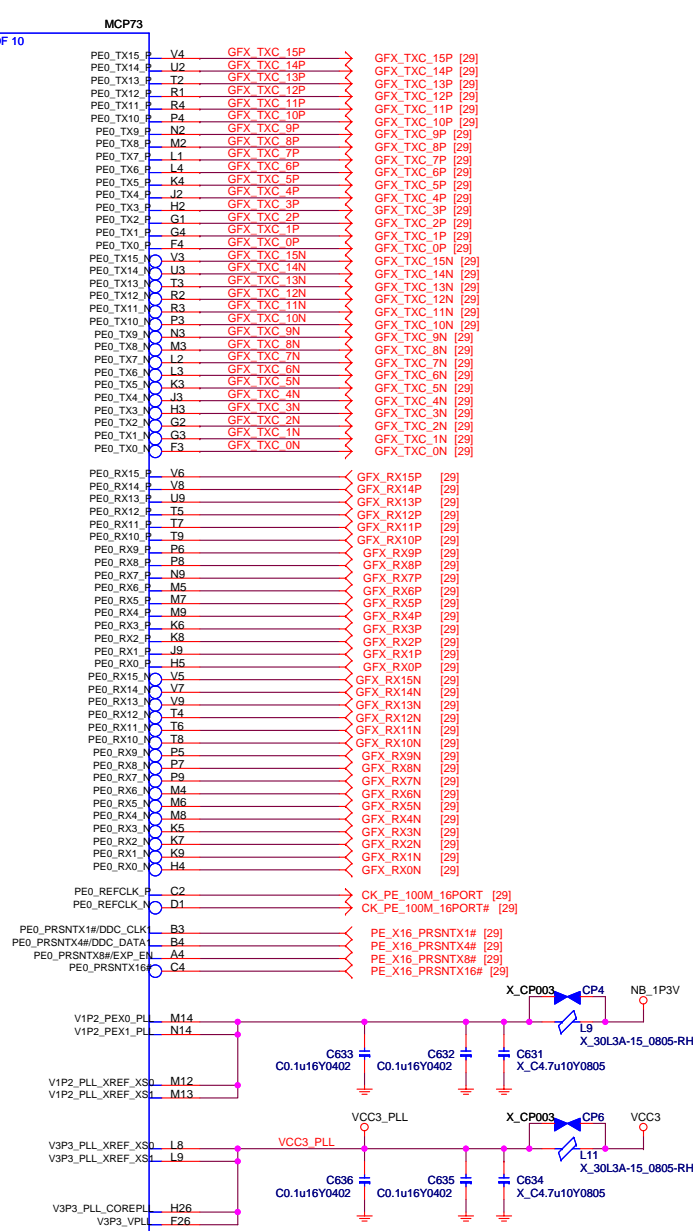
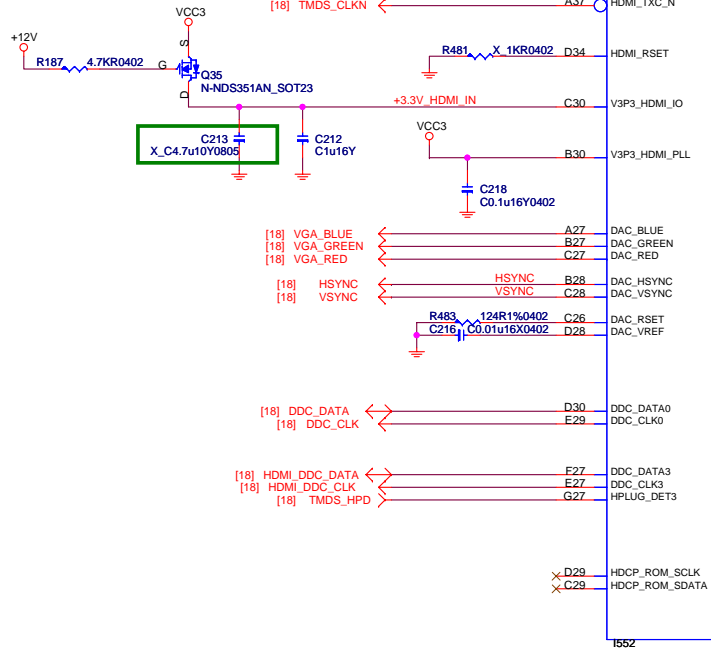


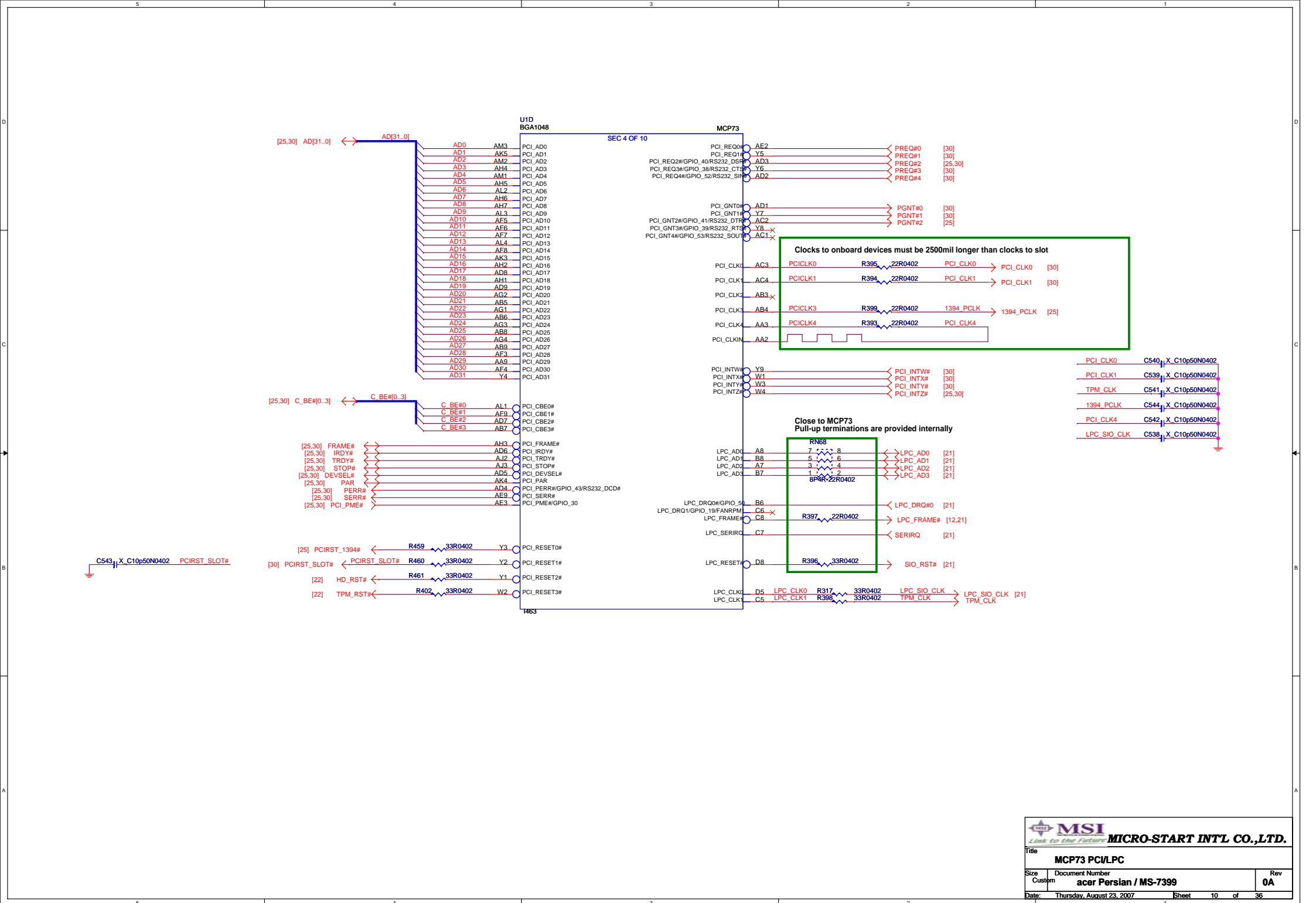


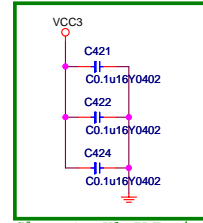
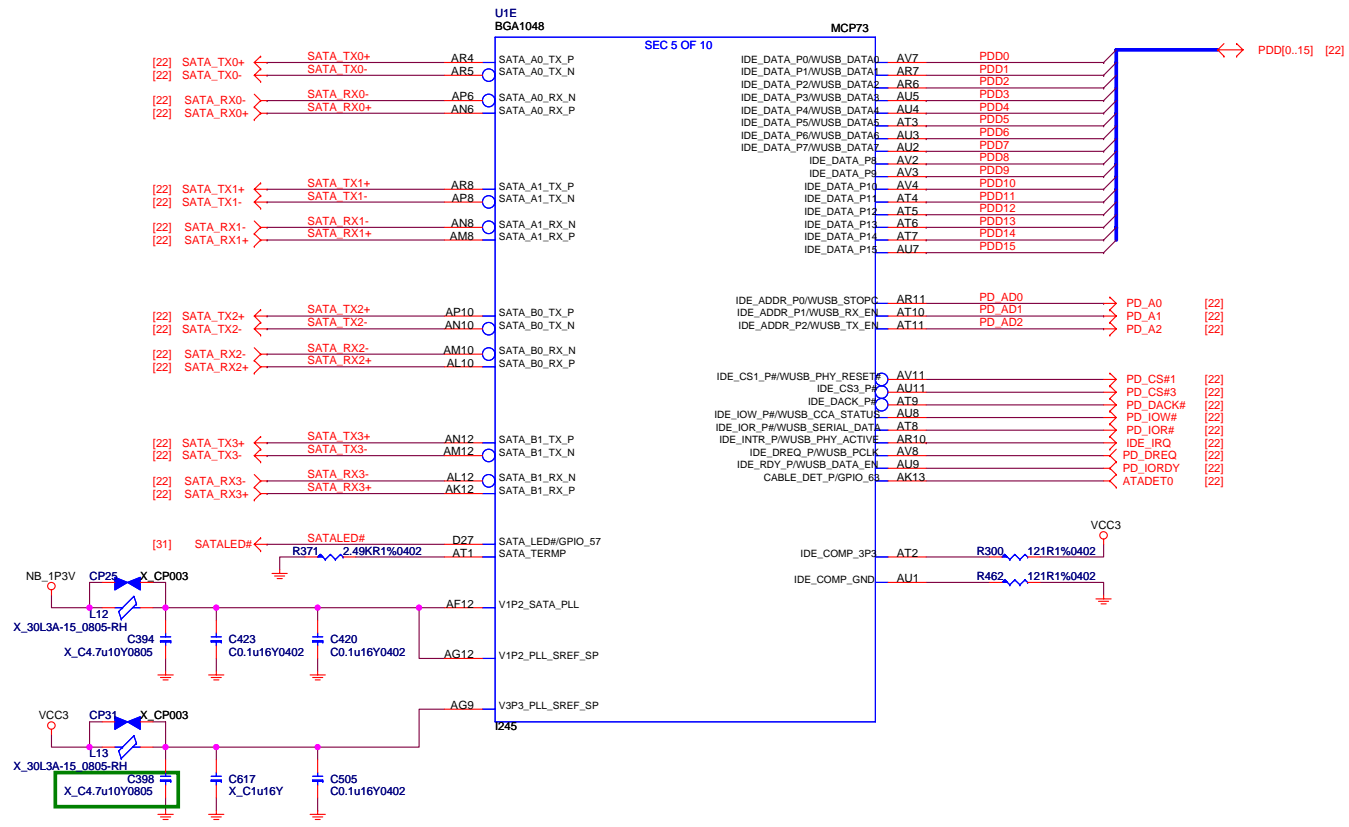
TMDS_00N	R796	X_0R0402	TMDS_00P
TMDS_01N	R797	X_0R0402	TMDS_01P
TMDS_02N	R798	X_0R0402	TMDS_02P
TMDS_CLKN	R799	X_0R0402	TMDS_CLKP



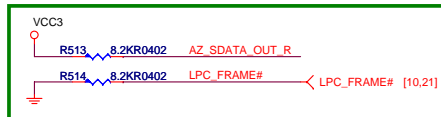
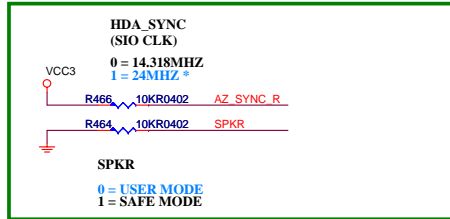
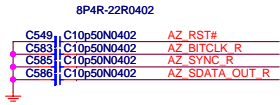
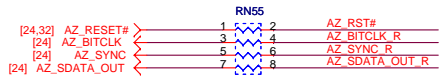
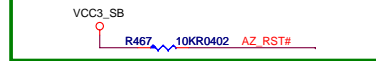
to prevent glitches during power-up



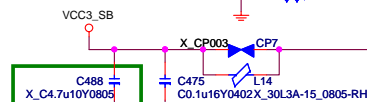
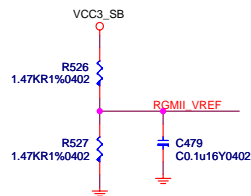




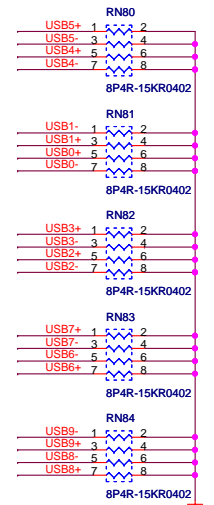
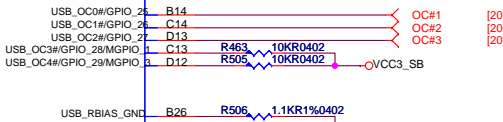
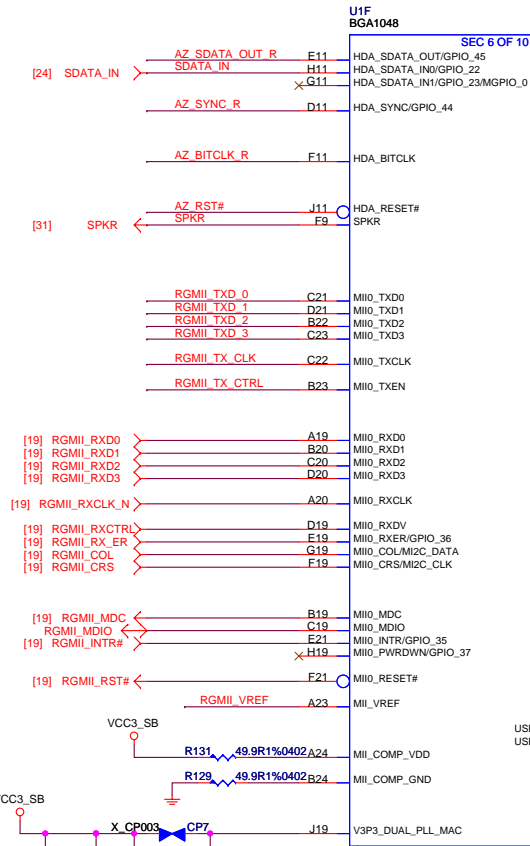
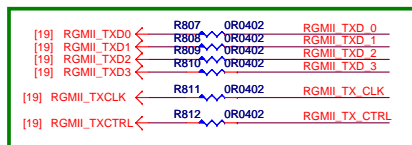
Strapping 10K ohm to VCC3\_SB: RGMII

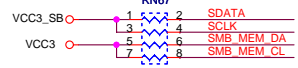
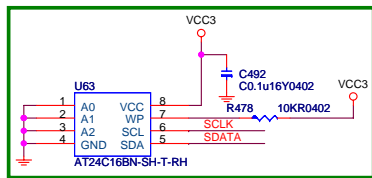


STRAP	HDA_SDOUT	LPC_FRAME
LPC BIOS	0	0
PCI BIOS	0	1
SPI BIOS	1	0
RESERVED	1	1

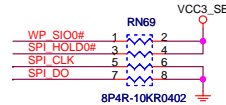
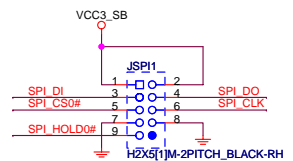
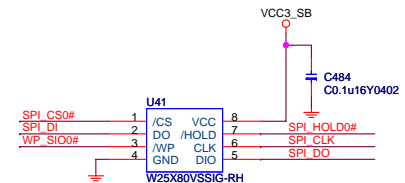
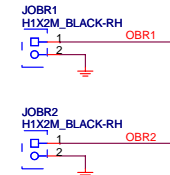
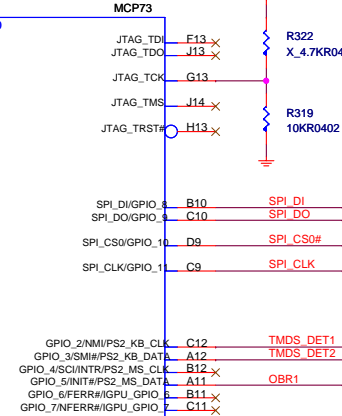
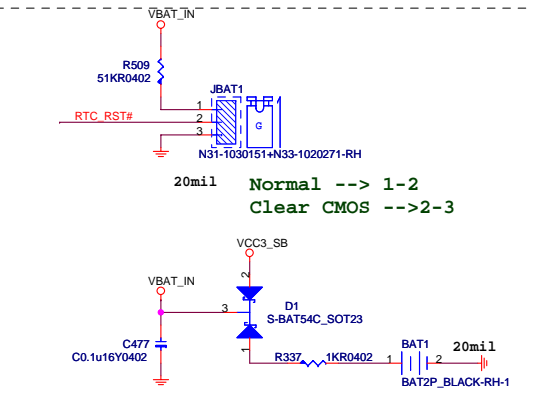
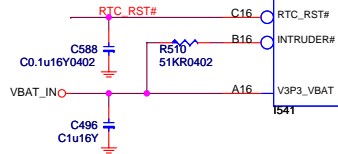
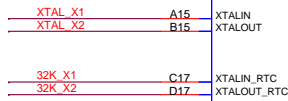
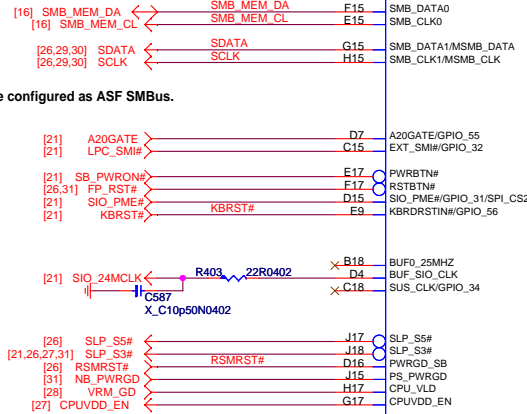
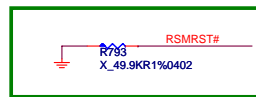
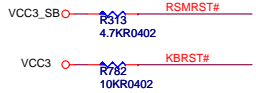


Close to U1



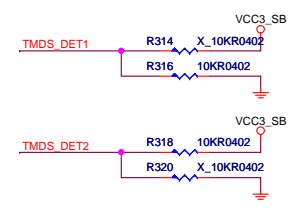


When SDATA/SCLK are not used, it can be configured as ASF SMBus.



MCP73 SPI CLK STRAP

STRAP	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1



HDMI/DVI Detect

	TMD5_DET1	TMD5_DET2
DVI	1	0
HDMI	0	1
N/A	0	0

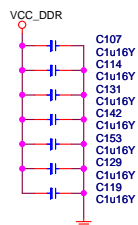
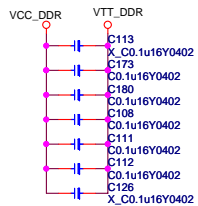
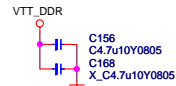
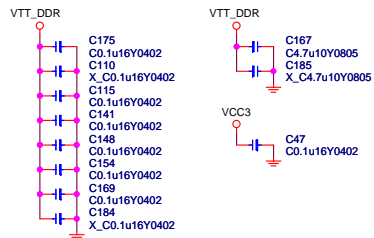




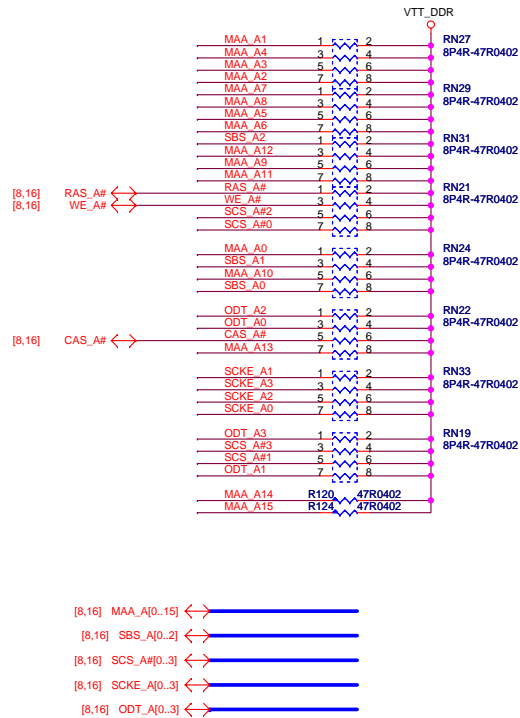




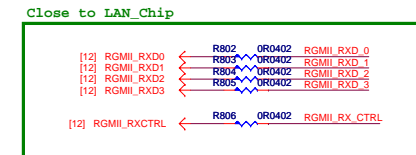
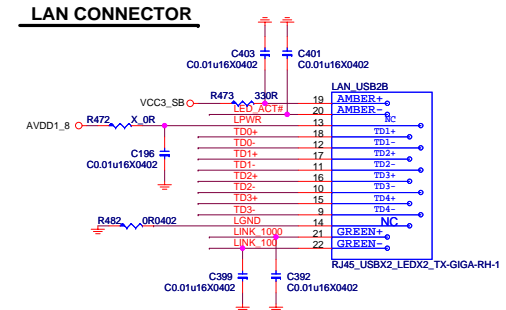
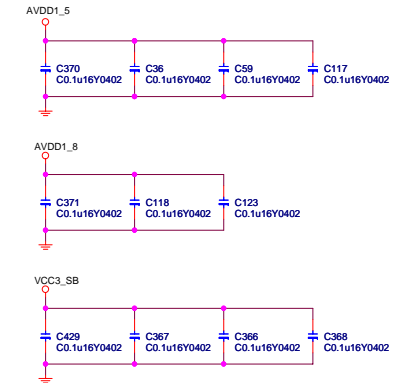
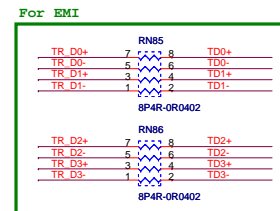
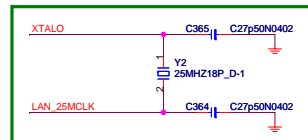
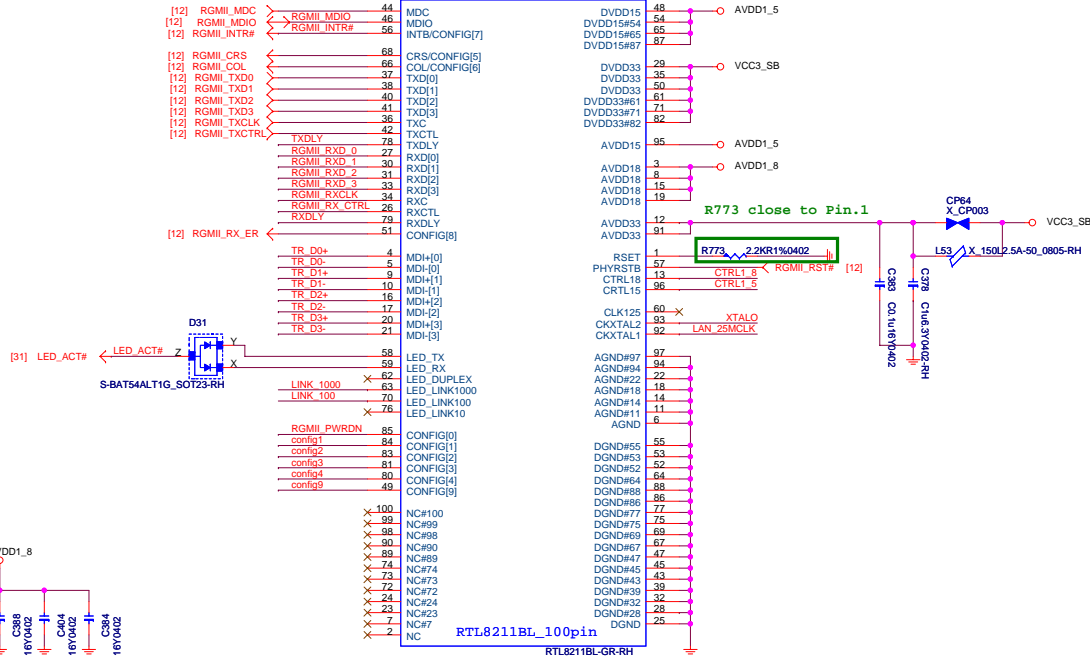
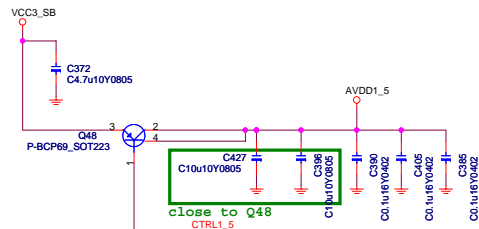
CHANNEL A VTT\_DDR  
DECOUPLING CAPS



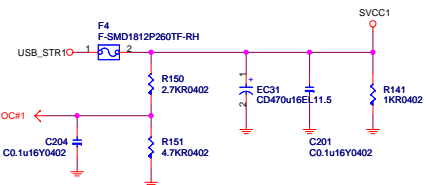
## DDR II TERMINATION



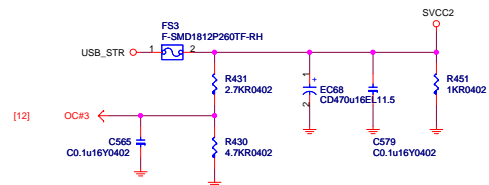




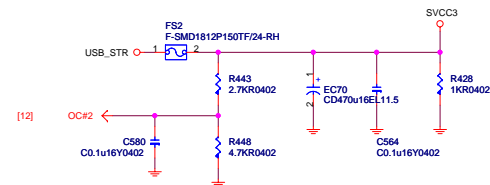
### POWER CIRCUIT FOR USB PORT 0,1,2,3



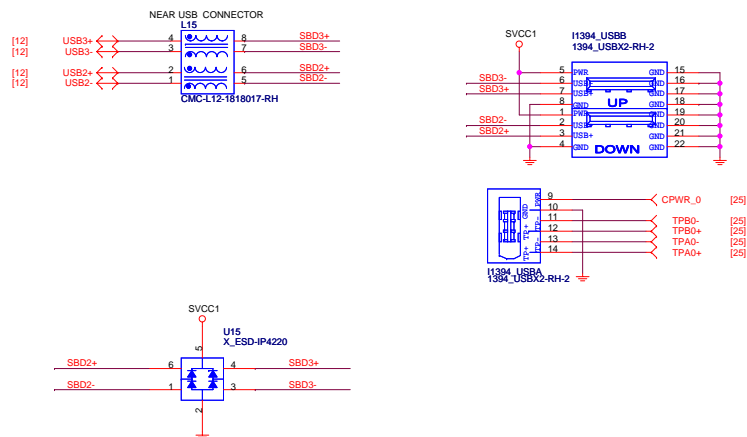
### POWER CIRCUIT FOR USB PORT 4,5,6,7



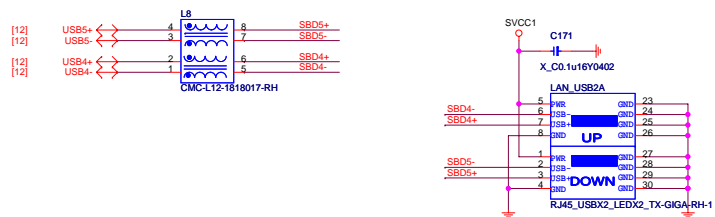
### POWER CIRCUIT FOR USB PORT 8,9



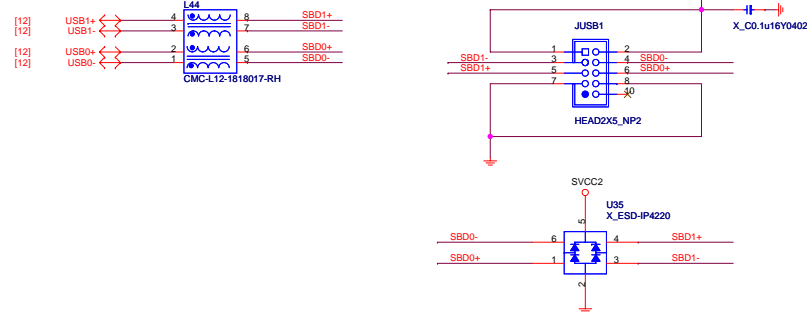
### REAR PANEL USB CONNECTOR FOR USB PORT 0,1



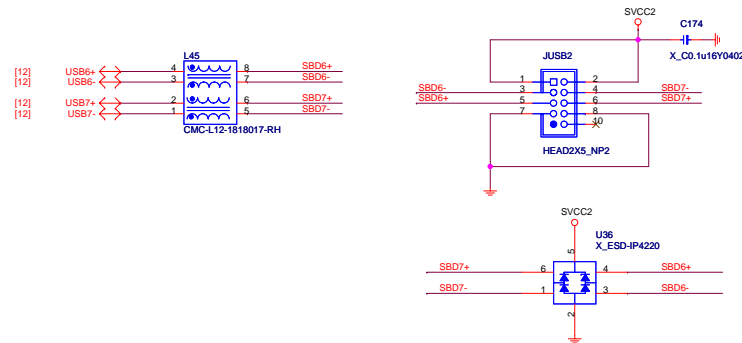
### REAR PANEL USB CONNECTOR FOR USB PORT 2,3



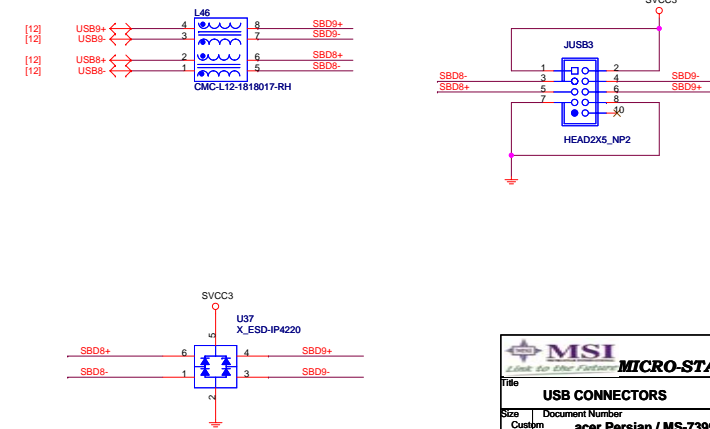
### FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



### FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



### USB CARD READER + IR MODULE FOR USB PORT 8,9





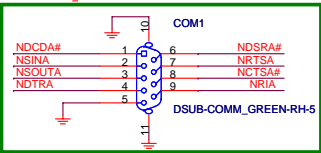
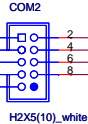
[11] PDD[0..15]  $\longleftrightarrow$



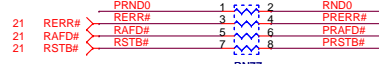
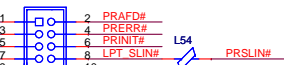
## CATM



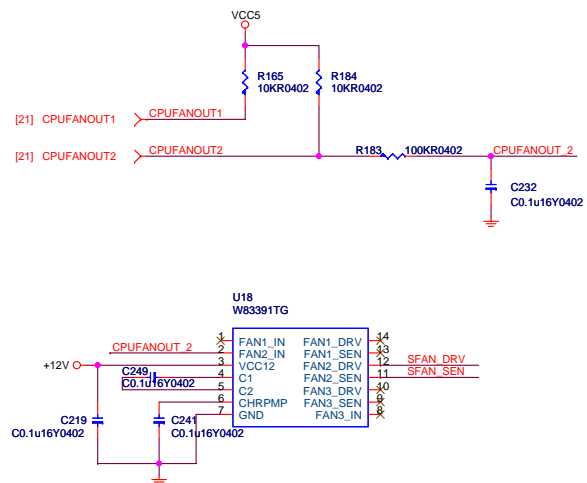
## C344.X C0.1u

[illegible]

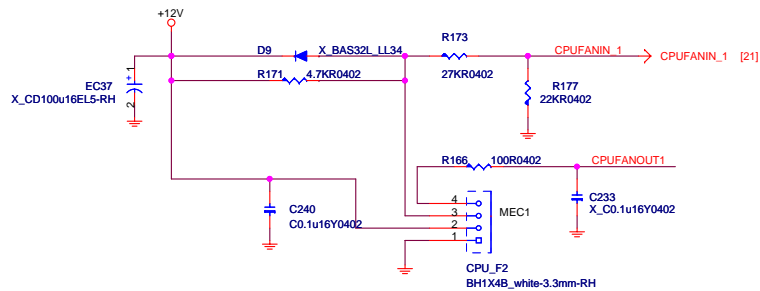
21 PRND[0..7]  $\longleftrightarrow$  PRND[0..7]



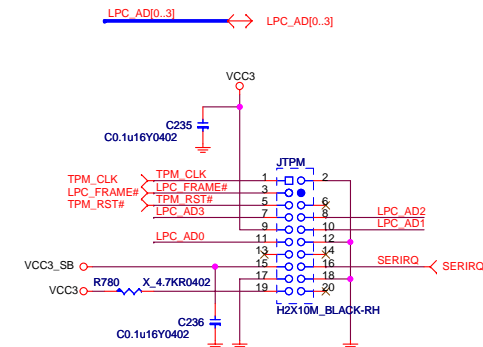
## PWM FAN CONTROL



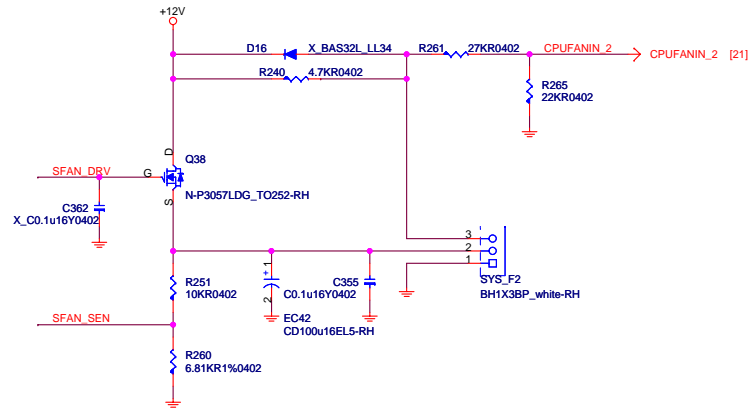
## CPU FAN



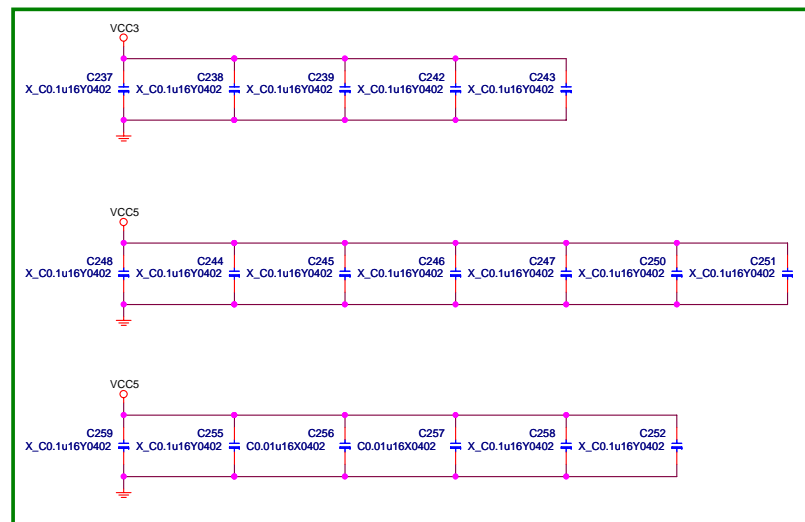
## TPM Header

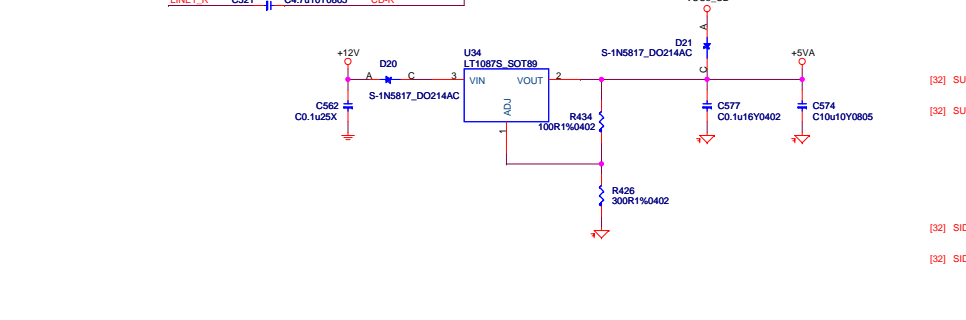
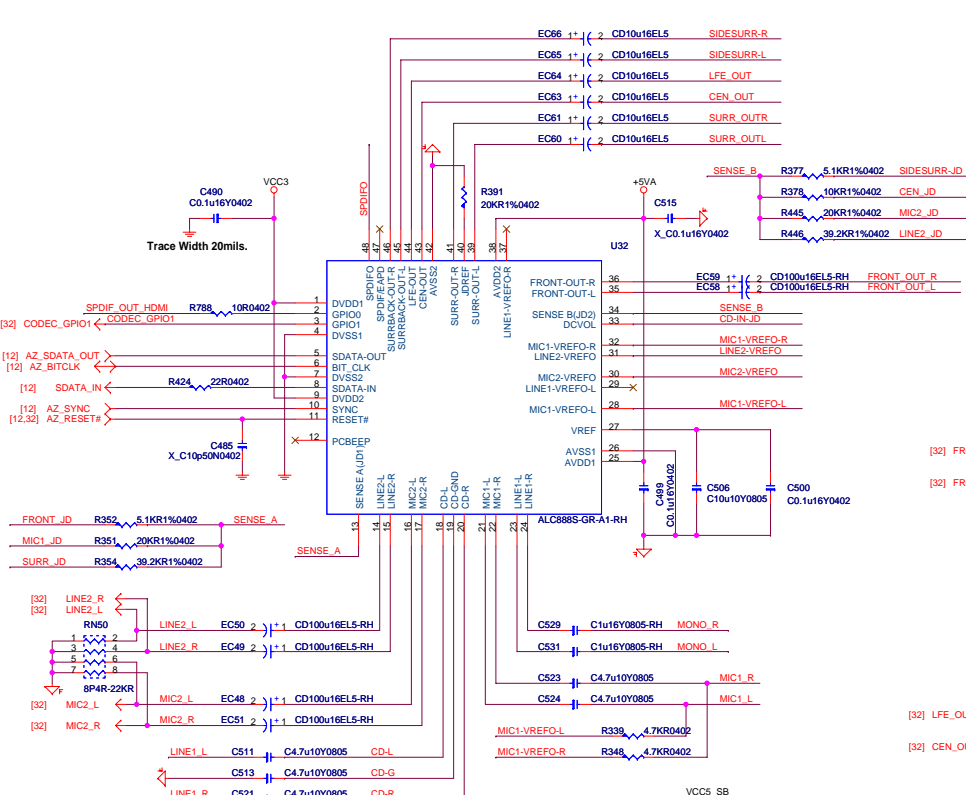


## SYS FAN

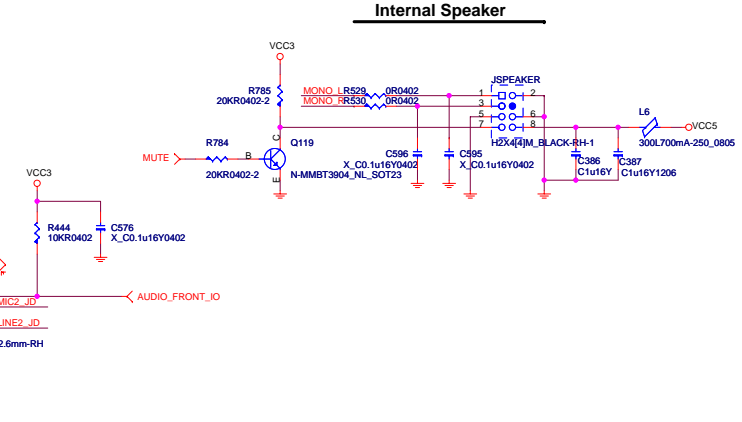
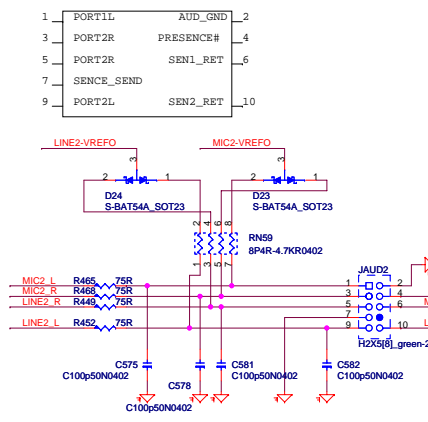


For EMI

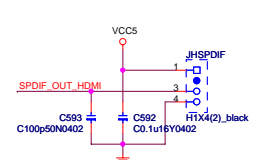




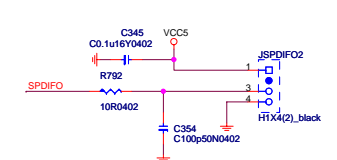
FRONT AUDIO PIN HEADER FOR AZALIA



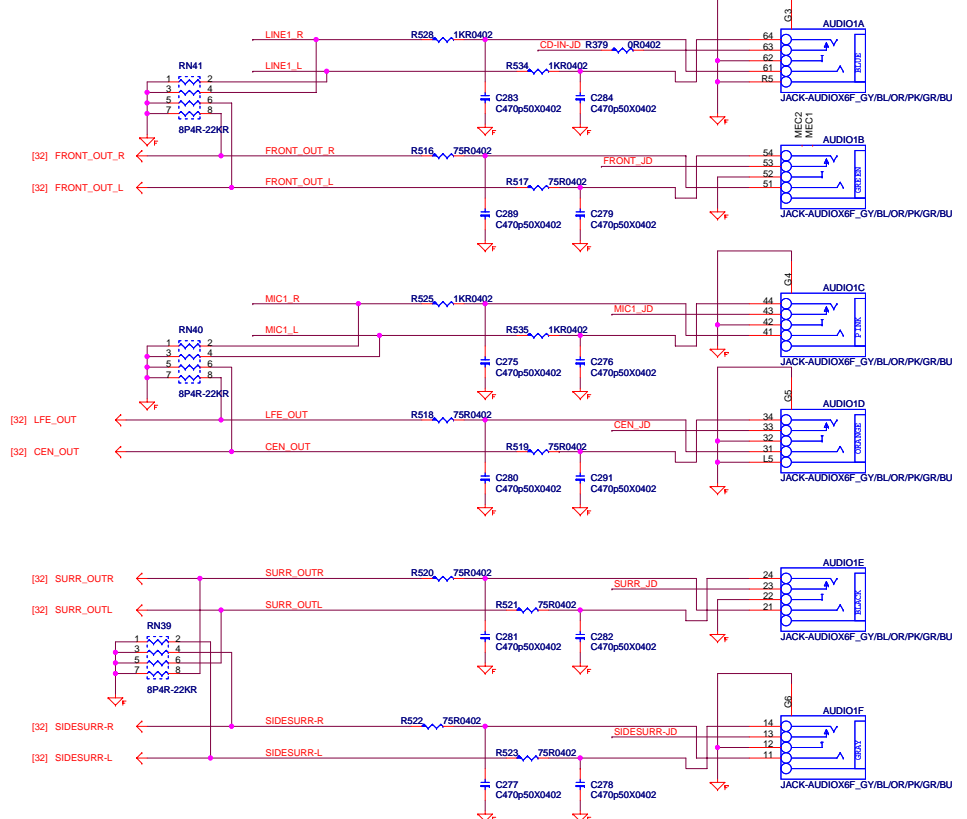
HDMI SPDIF HEADER



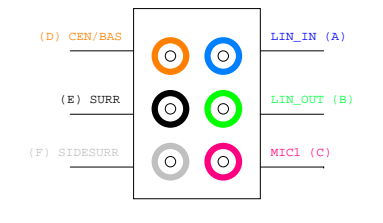
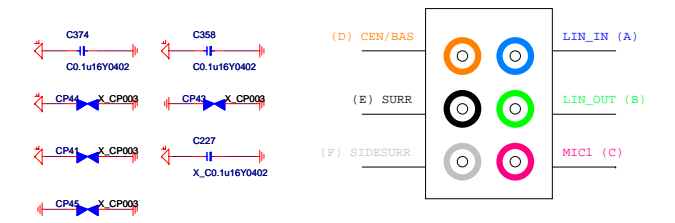
SPDIF HEADER



Rear audio jack

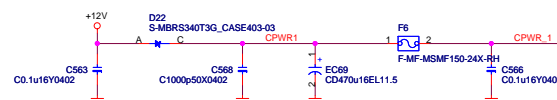
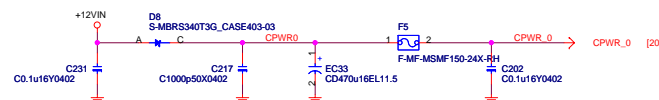
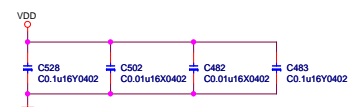
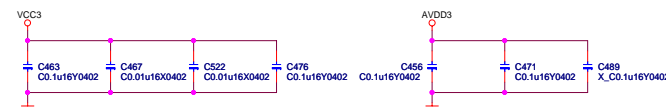


Internal Speaker



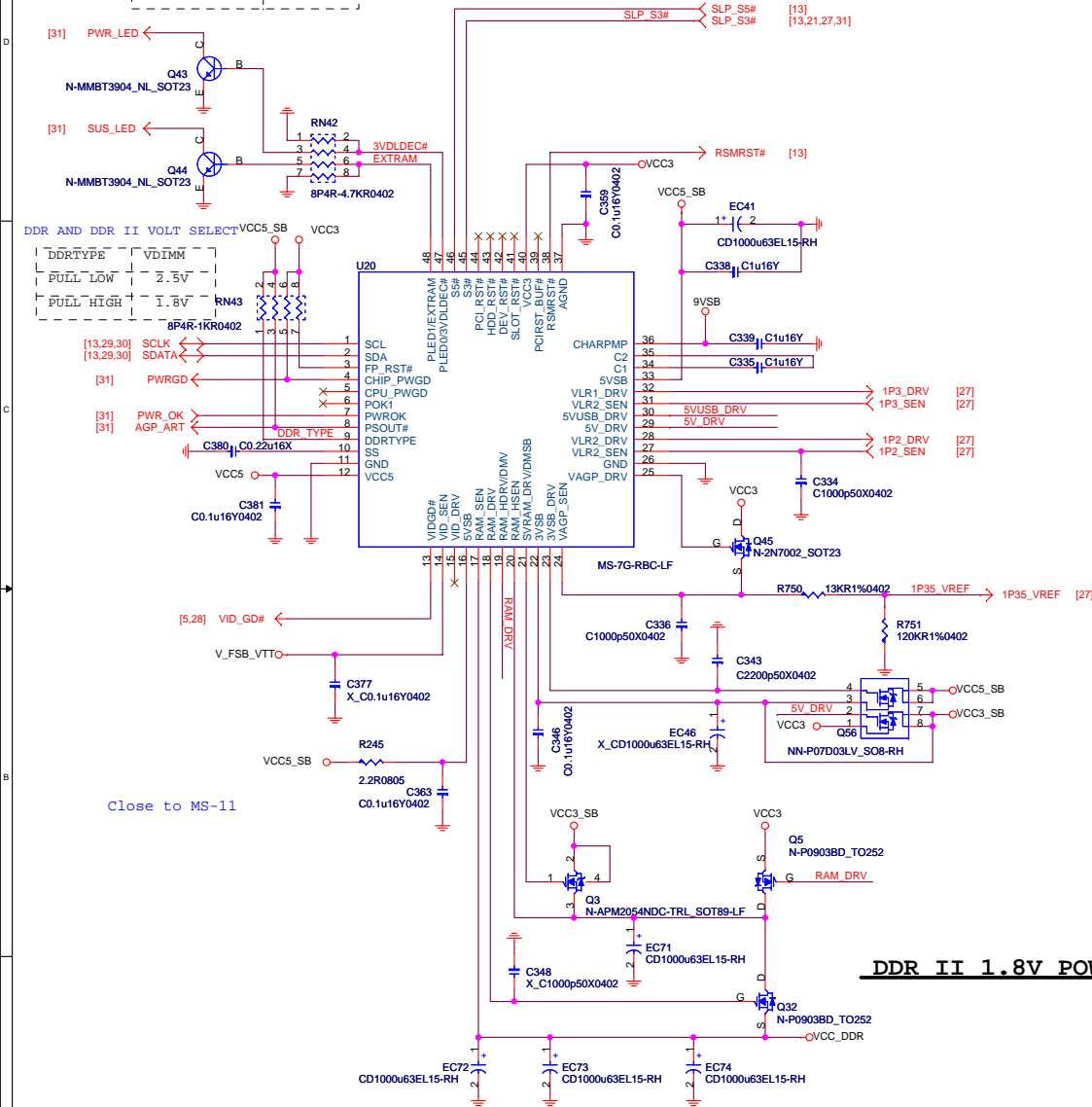


```
IDSEL = AD23
MASTER = PREQ#2/PGNT#2
PCI_INTZ#
```



3VSB MODE SELECT	
3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH



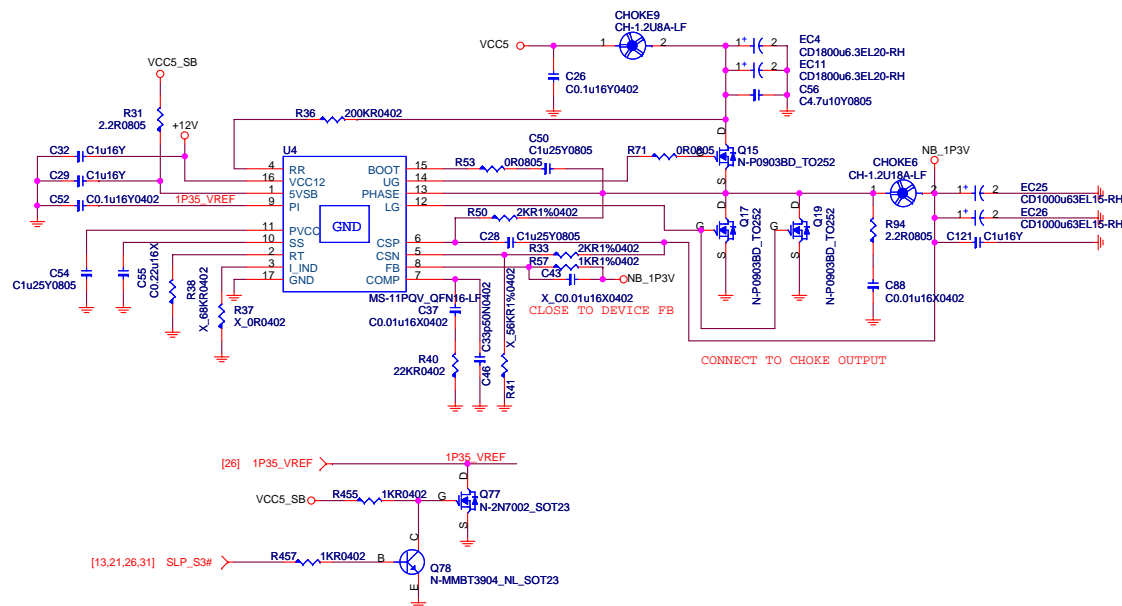
The schematic diagram illustrates a USB-to-serial interface circuit. It features two NPN transistors, Q62 (N-APM2054NDC-TRL\_SOT189-LF) and Q75 (N-P0903BD\_TO252), which act as level shifters. The circuit is powered by two 5V sources: 5V\_USB\_DRV and 5V\_DRV. Decoupling capacitors C228, C555, C573, C208, and C211 are used to filter noise. Pull-up resistors R201 and R202 are connected to the USB\_STR and USB\_STR1 signals. The serial interface is connected to the bases and collectors of the transistors. The USB\_STR signal is connected to the emitter of Q62 and the collector of Q75. The USB\_STR1 signal is connected to the emitter of Q75 and the collector of Q62. The serial interface is connected to the bases of Q62 and Q75. The serial interface is connected to the bases and collectors of the transistors. The USB\_STR signal is connected to the emitter of Q62 and the collector of Q75. The USB\_STR1 signal is connected to the emitter of Q75 and the collector of Q62. The serial interface is connected to the bases of Q62 and Q75.

## NB 1.3V CORE POWER

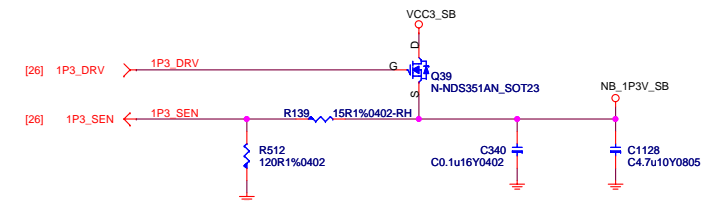
(1.3V--8.776A+V\_FSB\_VTT---5.6A=14.376)

The Ripple Current For V\_1P25\_CORE:  
 $Duty = (1.35V/5V) * (100\%/80\%) = 0.3375$  (Efficiency: 80%)  
 $I_{rms} = I_o * \{ [Duty * (1 - Duty)]^{0.5} \}$   
 $= 14.4 * \{ [0.27 * 0.73]^{0.5} \} = 6.393$  (A)

Rated Ripple Current (65 degree):  $1800mA * 2.3 * 2 = 8.28A > 6.393A$

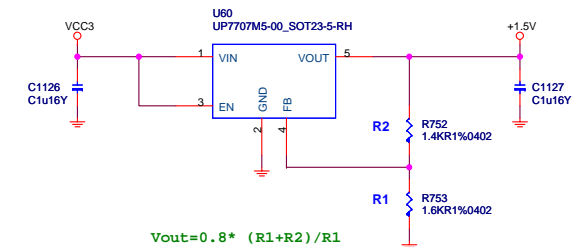


## NB 1.3VSB POWER 25mA

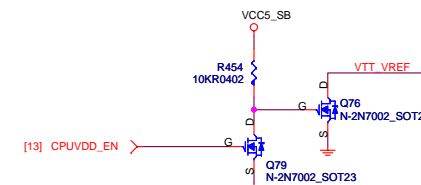
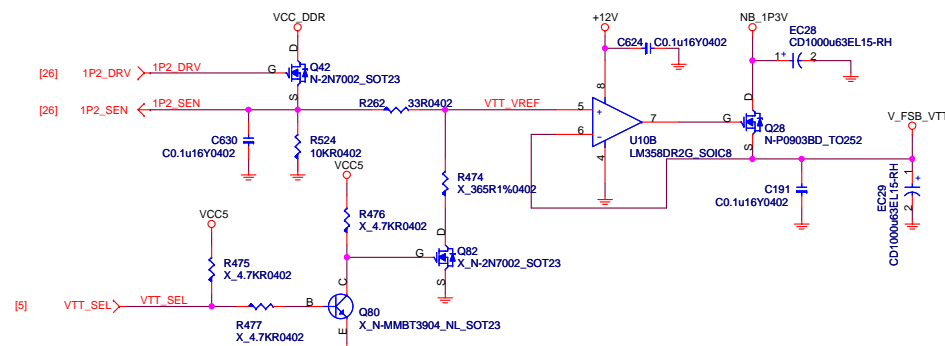


## +1.5V POWER

up7707: 600mA Low Dropout Linear Regulator

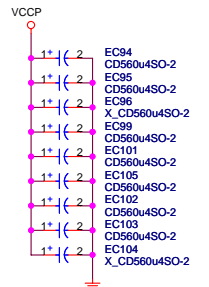
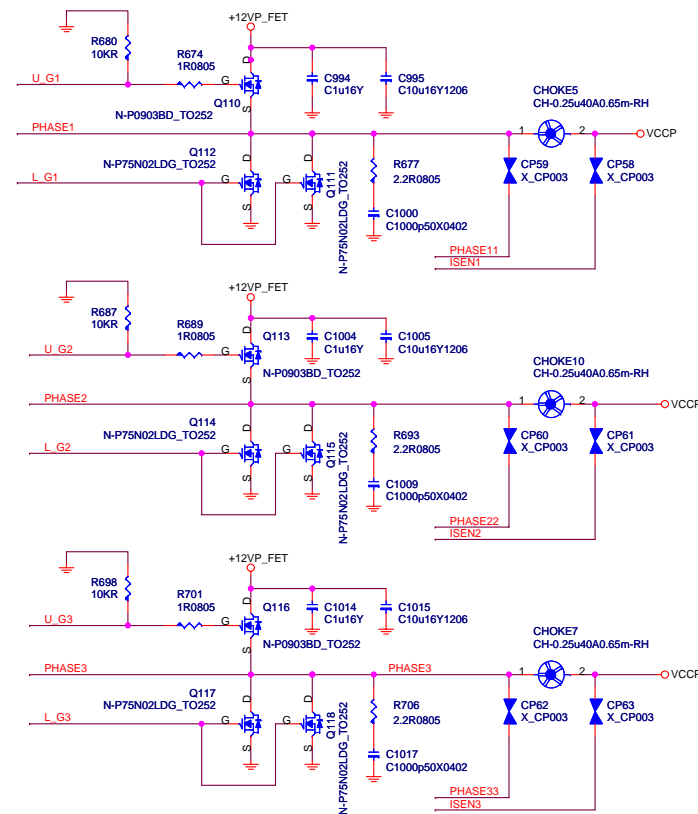
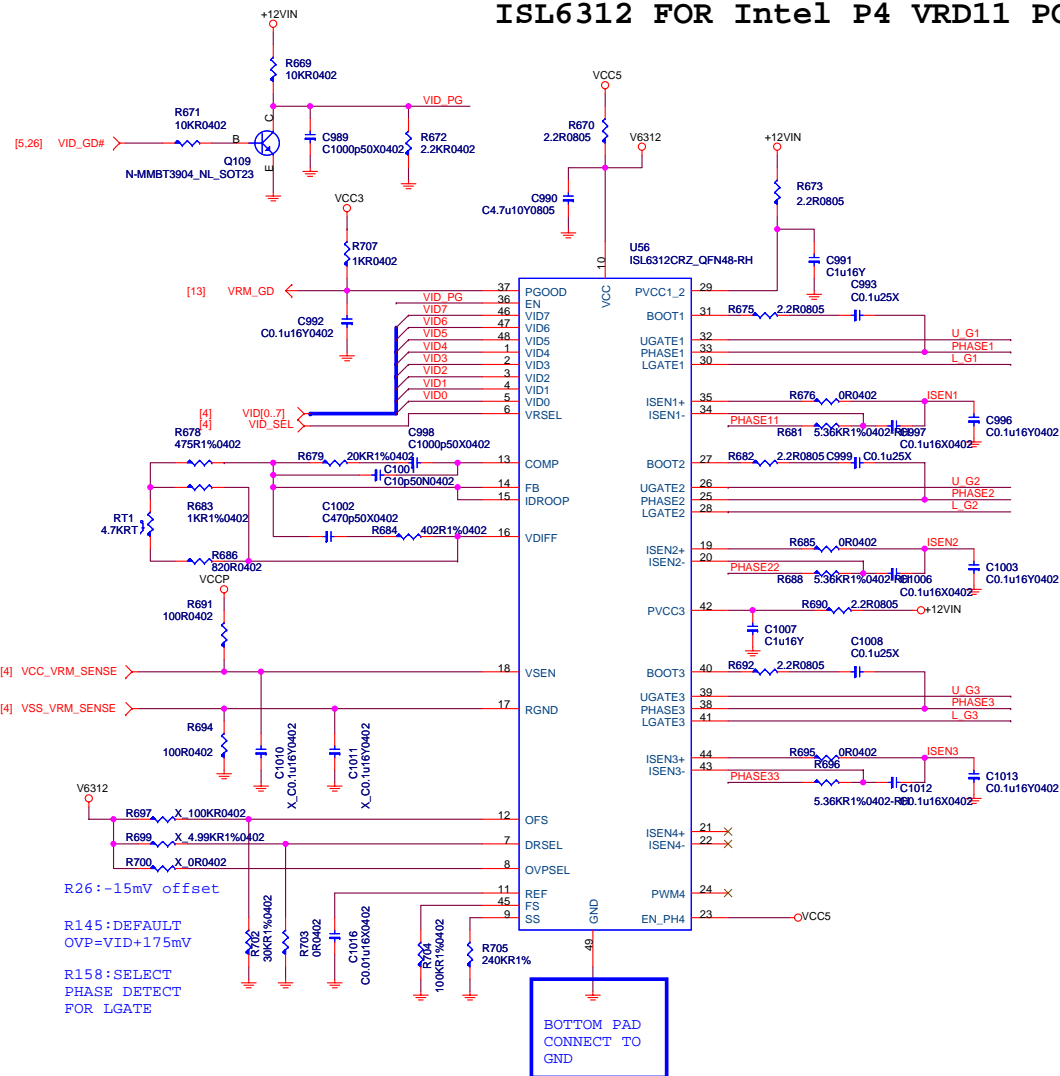


## CPU FSB VTT POWER

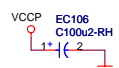


VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

## ISL6312 FOR Intel P4 VRD11 POWER CKT

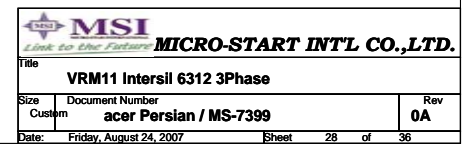
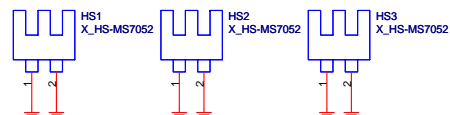
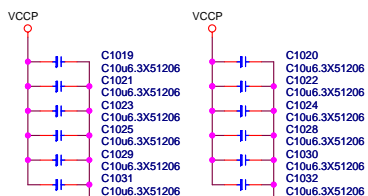


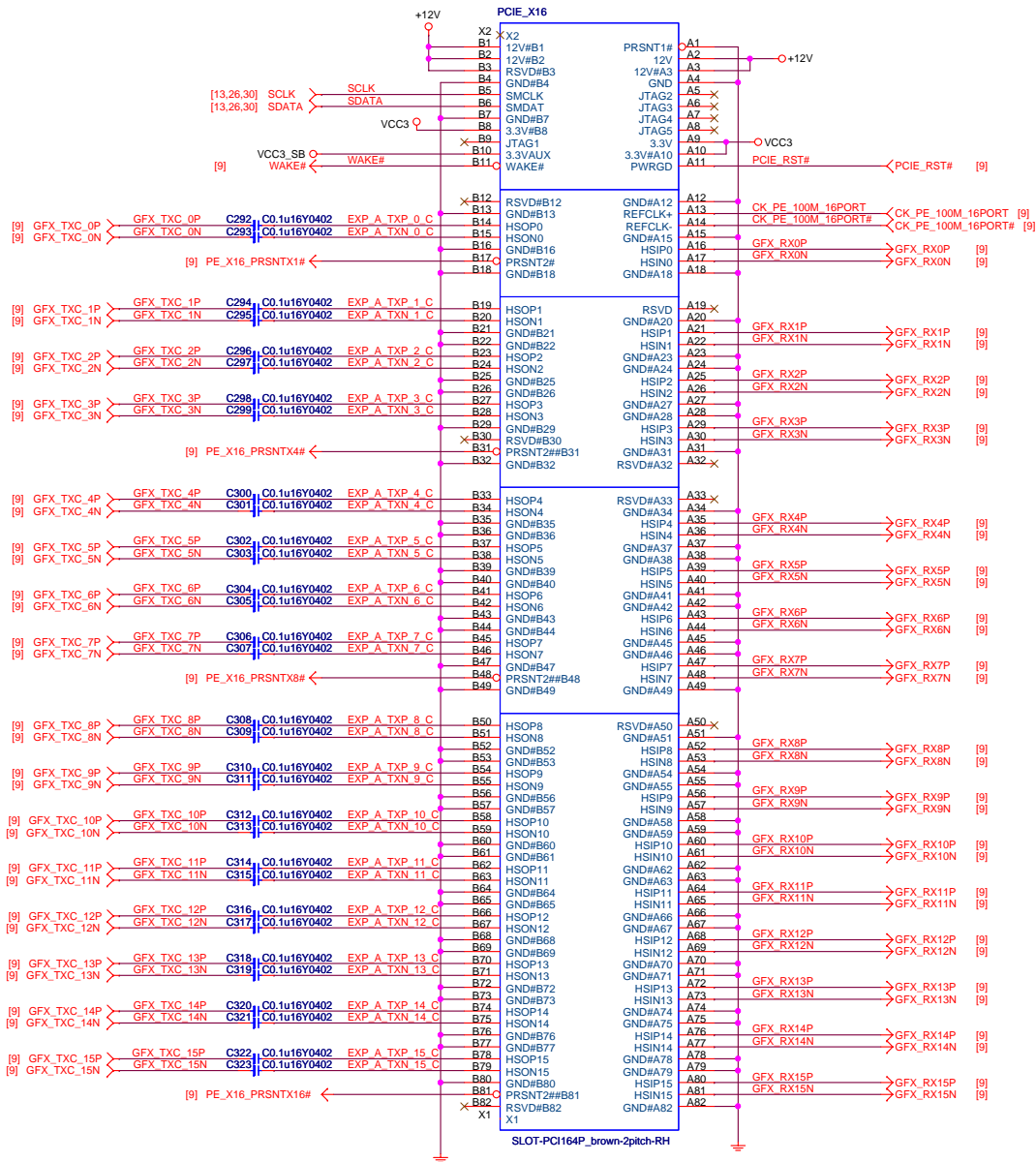
## SP Capacitors



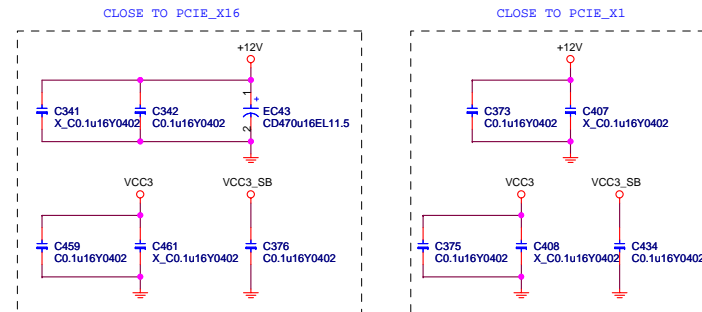
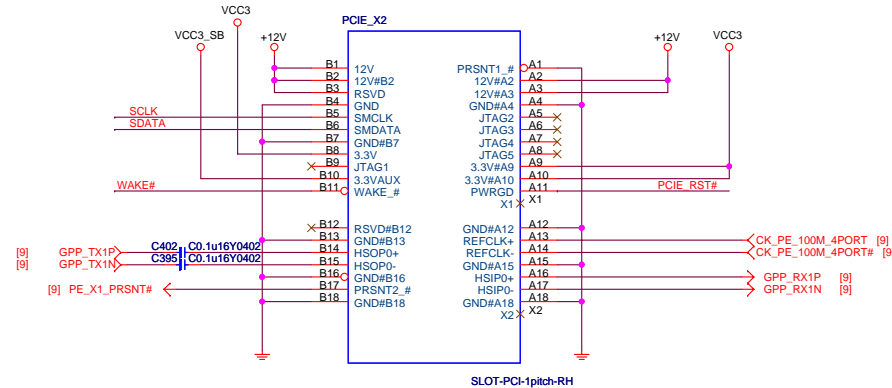
## CPU DECOUPLING CAPACITORS

Place these caps within socket cavity

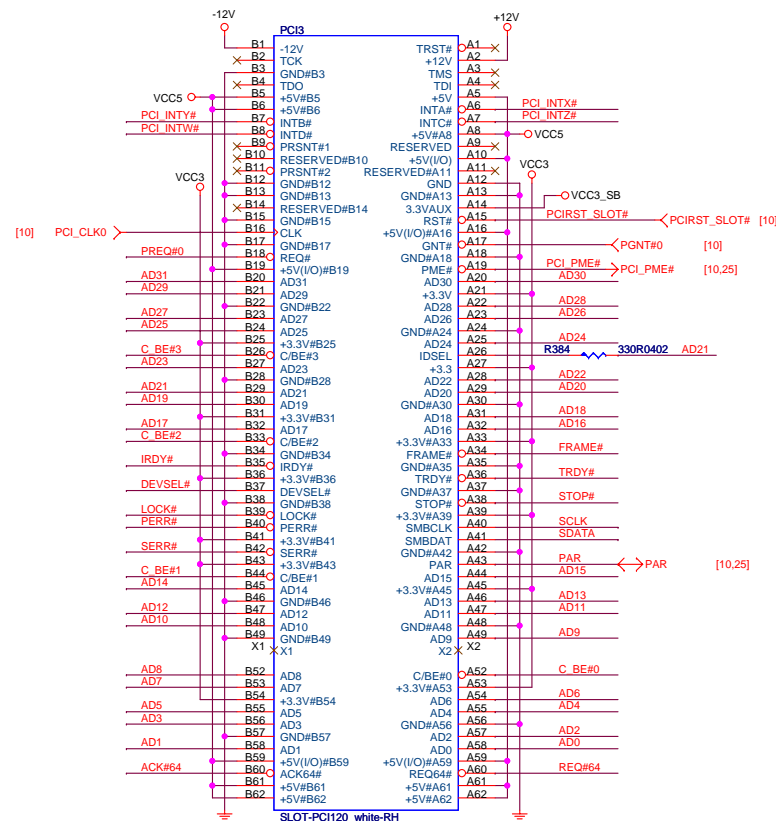




## PCI EXPRESS 1-PORT



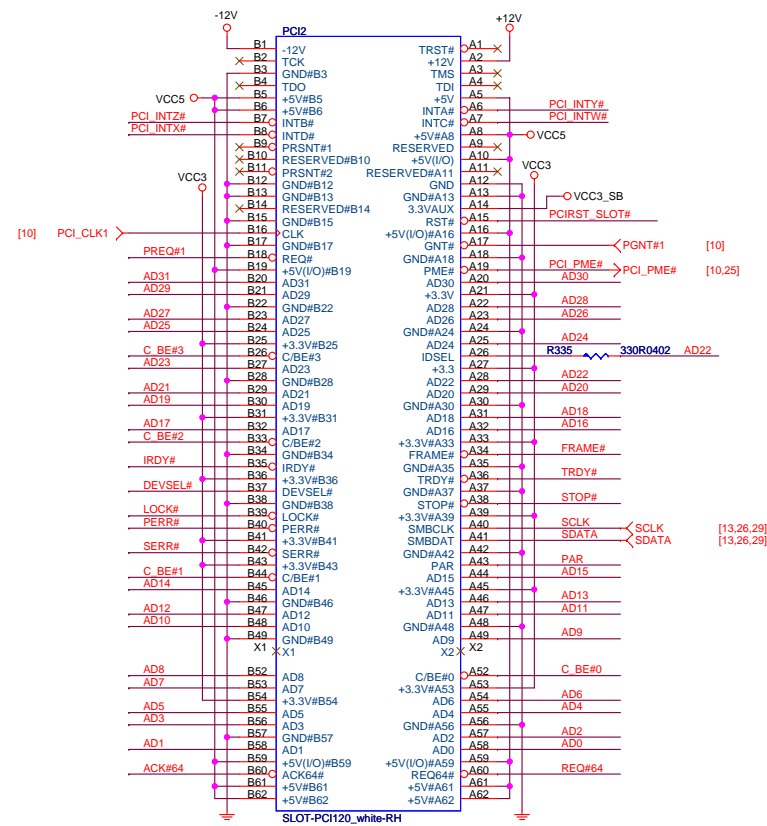
# PCI SLOT 1 (PCI VER: 2.3 COMPLY)



**IDSEL = AD21**  
**MASTER = PREQ#0**  
**PCI\_INTX#**

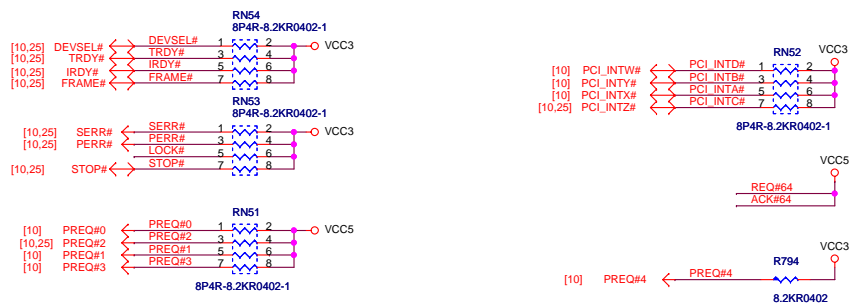
[10,25] AD[0..31] ← AD[0..31]  
 [10,25] C\_BE[0..3] ← C\_BE[0..3]

# PCI SLOT 2 (PCI VER: 2.3 COMPLY)

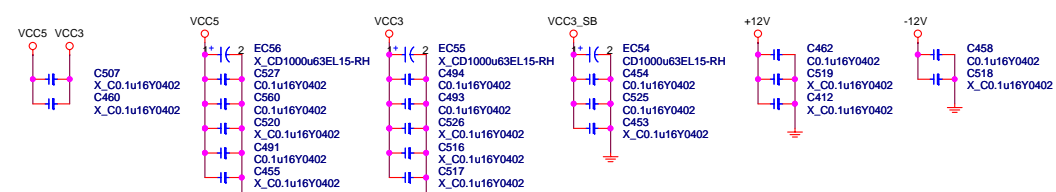


**IDSEL = AD22**  
**MASTER = PREQ#1**  
**PCI\_INTY#**

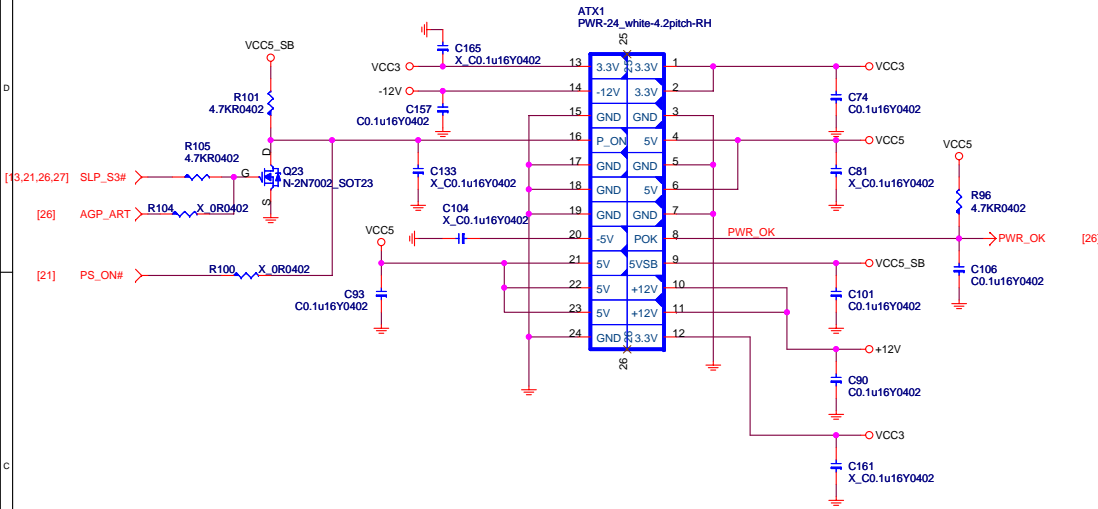
## PCI PULL-UP / DOWN RESISTORS



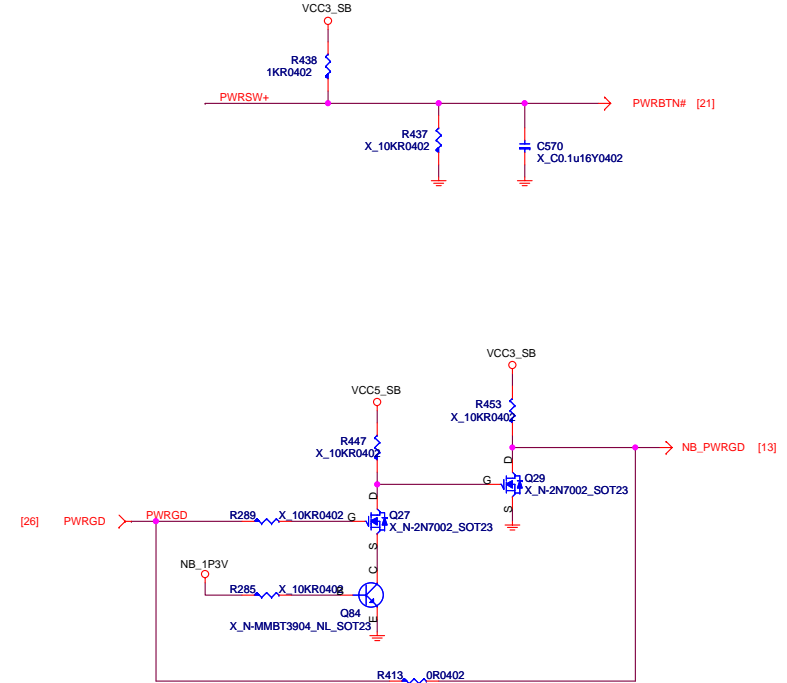
## PCI SLOT DECOUPLING CAPACITORS



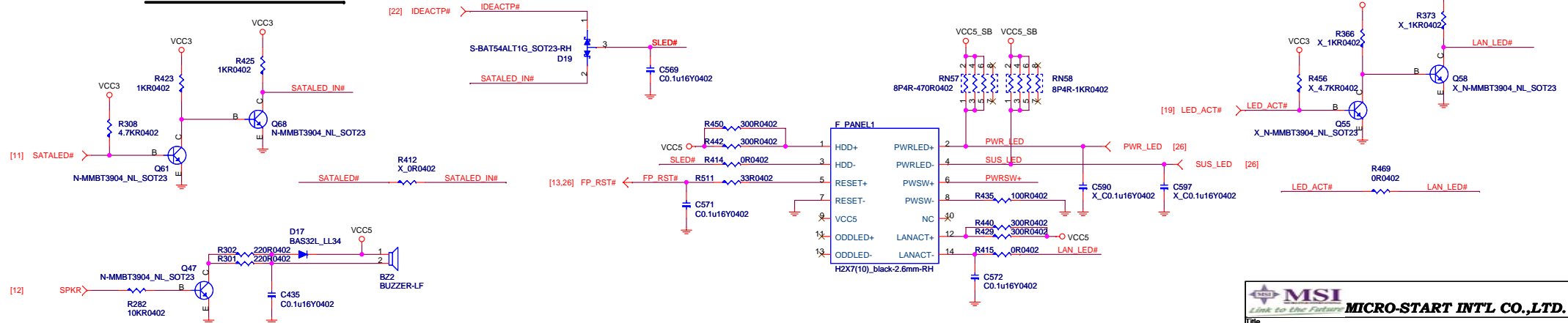
## ATX CONNECTOR



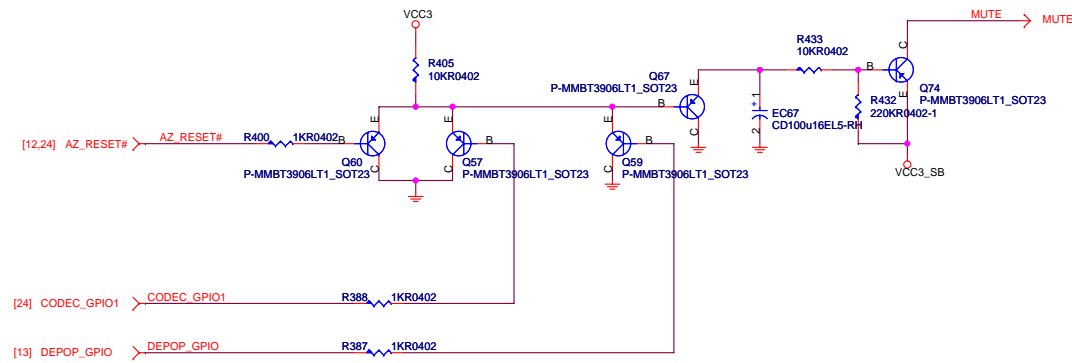
## POWER BUTTON



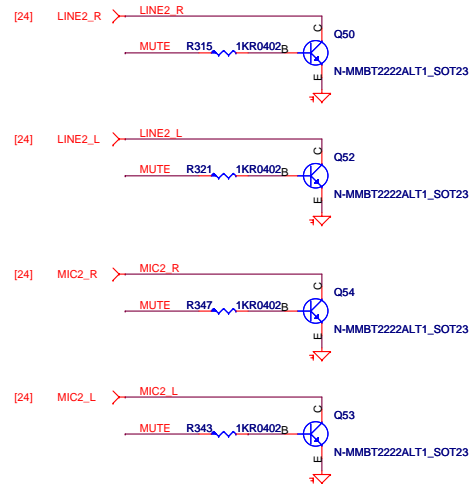
## acer Front Panel Connector



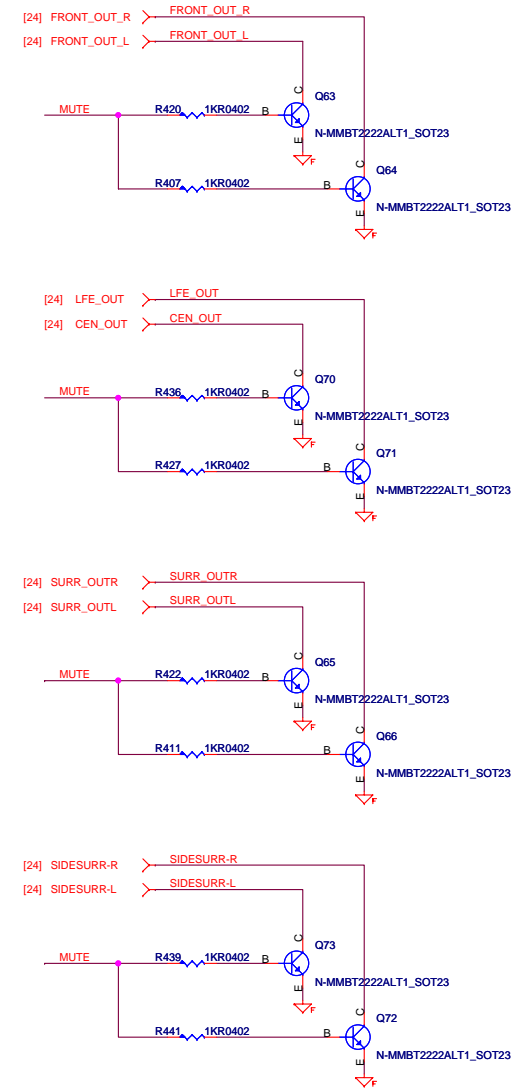
## Audio De-Pop Control Circuit



## Front Audio Port De-Pop Circuit

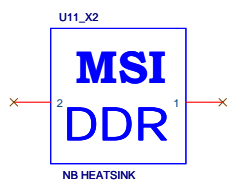


## Rear Audio Port De-Pop Circuit

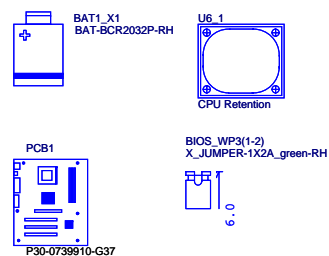




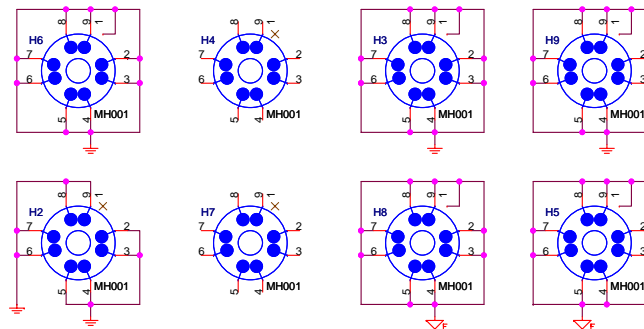
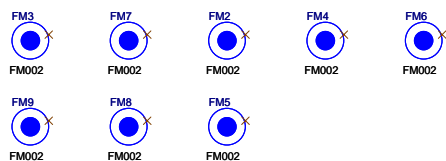
## HEAT SINK

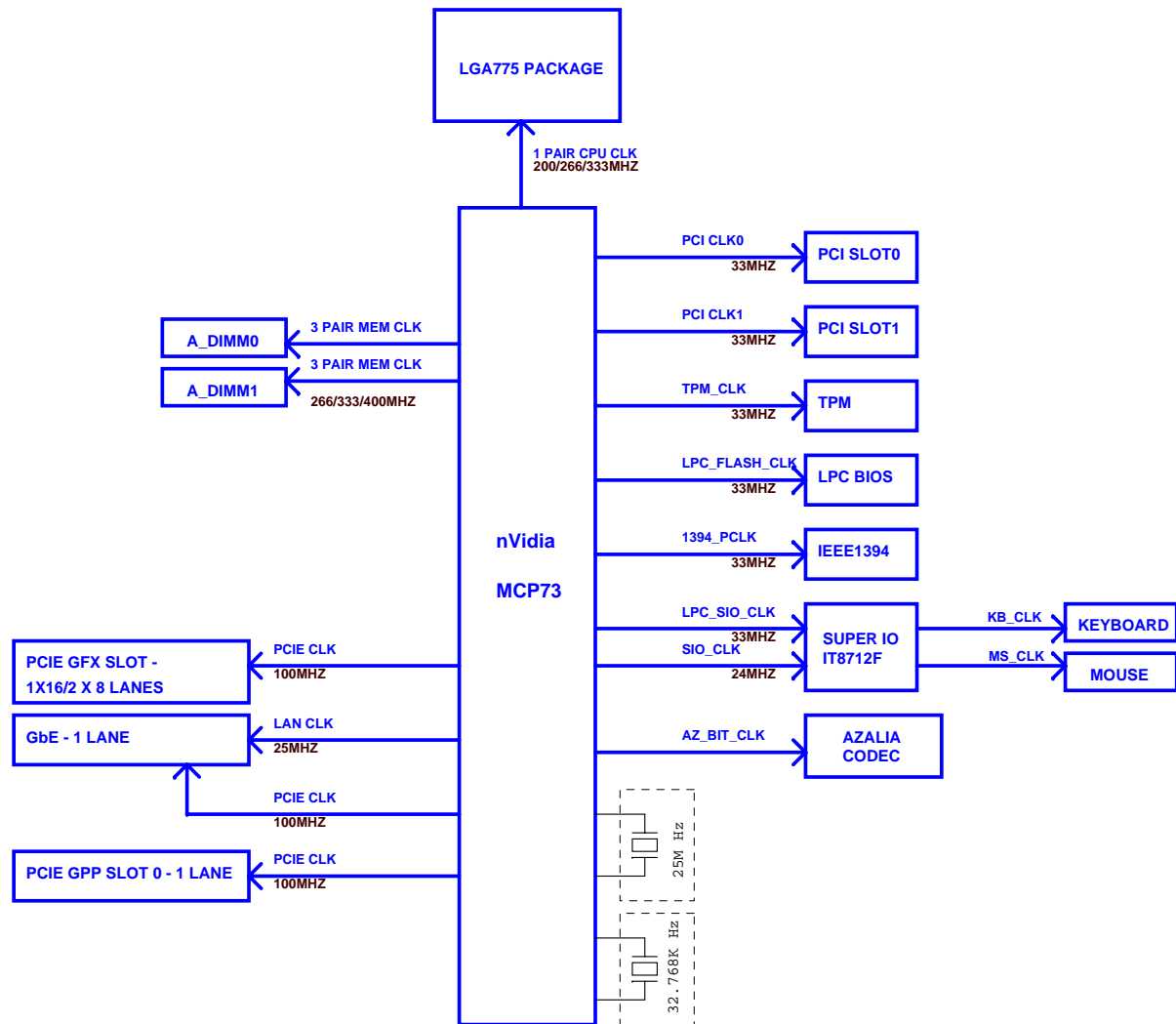


## MANUAL PART

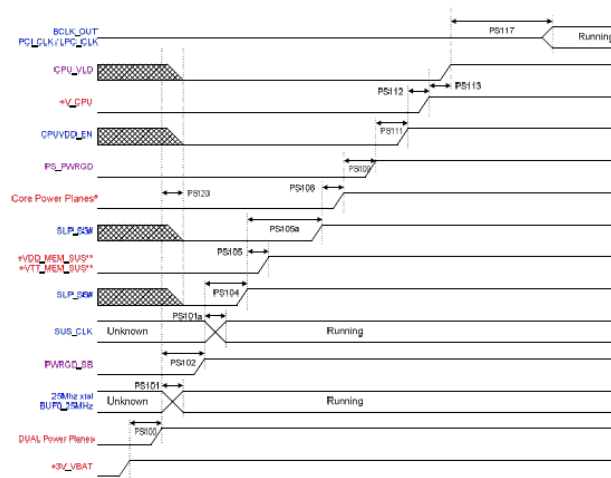


## Optics Orientation Holes







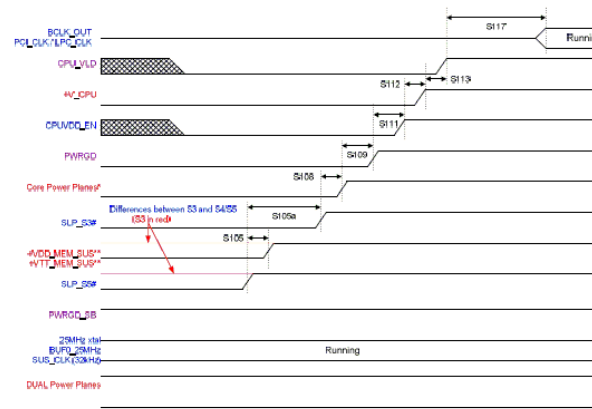


**Power Planes in Red** MCP73 output signals in Blue Motherboard generated signals in Purple

\* Core Planes include:  
All power planes without \_DUAL or \_SUS in the name except:  
CPU Core Power Plane

\*\* DDR2 Memory Power Planes:  
VDD = 1.8V  
VTT = 0.9V

MCP73 G3-to-S0 Power-Up Sequence

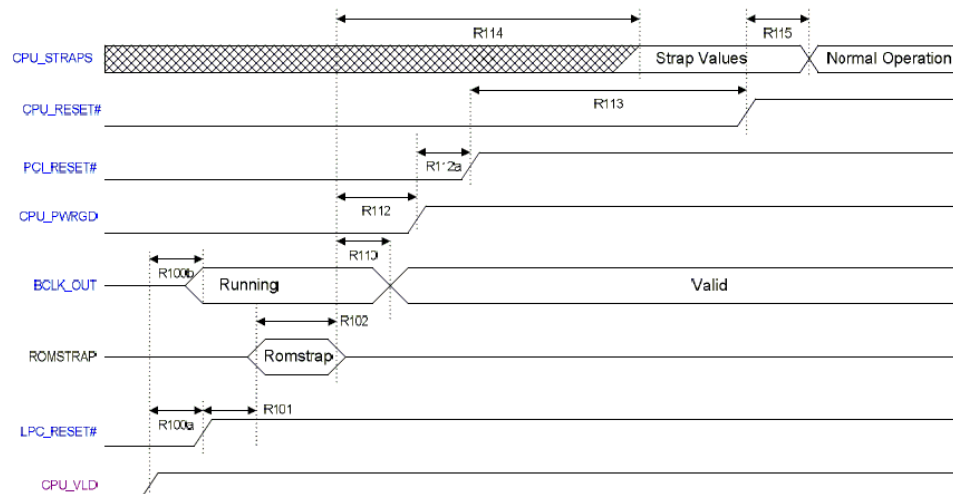


**Power Planes in Red** MCP73 output signals in Blue Motherboard generated signals in Purple

\* Core Planes include:  
All power planes without \_DUAL or \_SUS in the name except:  
- CPU Core Power Plane

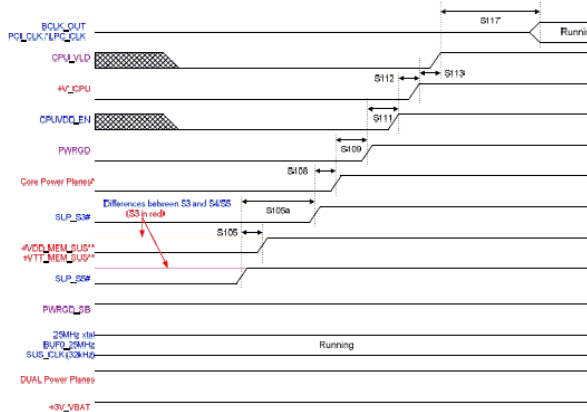
\*\* DDR2 Memory Power Planes:  
VDD = 1.8V  
VTT = 0.9V

MCP73 S3/S4/S5 to S0 Power Resume Sequence



**MCP73 output signals in Blue** Motherboard generated signals in Purple

MCP73 Cold Reset Power-Up Sequence



**Power Planes in Red** MCP73 output signals in Blue Motherboard generated signals in Purple

\* Core Planes include:  
All power planes without \_DUAL or \_SUS in the name except:  
- CPU Core Power Plane

\*\* DDR2 Memory Power Planes:  
VDD = 1.8V  
VTT = 0.9V

MCP73 S3/S4/S5 to S0 Power Resume Sequence